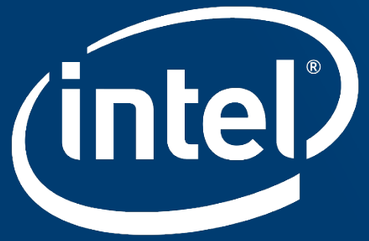


WHITLEY/CEDAR ISLAND PLATFORM MESSAGE OF THE WEEK [MOW] UPDATE

Intel Corporation
Data Center Platform Application Engineering
WW19 2020
Document ID: 575523
Intel Confidential

Legal Disclaimer

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at Intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Warning: Altering PC clock or memory frequency and/or voltage may (i) reduce system stability and use life of the system, memory and processor; (ii) cause the processor and other system components to fail; (iii) cause reductions in system performance; (iv) cause additional heat or other damage; and (v) affect system data integrity. Intel assumes no responsibility that the memory, included if used with altered clock frequencies and/or voltages, will be fit for any particular purpose. Check with memory manufacturer for warranty and additional details.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit http://www.intel.com/performance.

Cost reduction scenarios described are intended as examples of how a given Intel- based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Intel® AMT should be used by a knowledgeable IT administrator and requires enabled systems, software, activation, and connection to a corporate network. Intel AMT functionality on mobile systems may be limited in some situations. Your results will depend on your specific implementation. Learn more by visiting Intel® Active Management Technology.

Intel is a sponsor and member of the Benchmark XPRT Development Community, and was the major developer of the XPRT family of benchmarks. Principled Technologies is the publisher of the XPRT family of benchmarks. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel, Intel® Optane™, Xeon, and the Intel logo are trademarks of Intel Corporation in the U. S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Contents

ENABLING

ICE LAKE SAMPLES SENSITIVITY TO VCCSA - UPDATES

Ice Lake Samples Sensitivity to Vccsa - Updates

- Intel is seeing DC cycling failures with a small number of HCC ES1/ES2 parts. Typical failure signature is a DC cycling hang with **BL_REQ_RTID_TABLE_MISS** error. Failure is due to Vccsa sensitivity during reset, as an insufficient level of guardbanding was applied to ES manufacturing, leading to the issue seen.
- This issue is not expected to impact the board design.
- As the sensitivity occurs at boot time, we do not expect to have a work-around for HCC ES1/ES2. Since this sensitivity only occurs at boot time, Intel recommends that parts exhibiting this sensitivity to be re-allocated for non DC cycling activities.
- A fix has been identified to address the source of this sensitivity. This fix will be implemented starting with XCC ES1 & all subsequent Ice Lake HCC/XCC sample/production releases.

INTEL® SPEED SELECT TECHNOLOGY COMPLIANCE TEST FOR ICE LAKE AND COOPER LAKE

Intel Speed Select Technology – Enabling efforts

Intel® Speed Select Technology feature: HOW TO

- Avoid customer from trying various knobs in BIOS to use SST features.

Collaterals ready at RDC doc id 621725:-

Intel® Speed Select Technology (Intel® SST) for Intel® Xeon® Processor (Ice Lake and Cooper Lake) Compliance Test Guide for Linux* OS

Unique ID 621725 | **File Size:** 1.04 MB | **CCL Usage Type:** Targeted

Last Updated: 04/30/2020 | **File Type:** PDF File | **Version:** 0.4

Content Type: Guides

Intel® Speed Select Technology (Intel® SST) for Intel® Xeon® Processor (Ice Lake and Cooper Lake) Compliance Test Guide for Linux* OS

Link to Compliance Test Demonstration:-

http://10.5.250.47:8000/

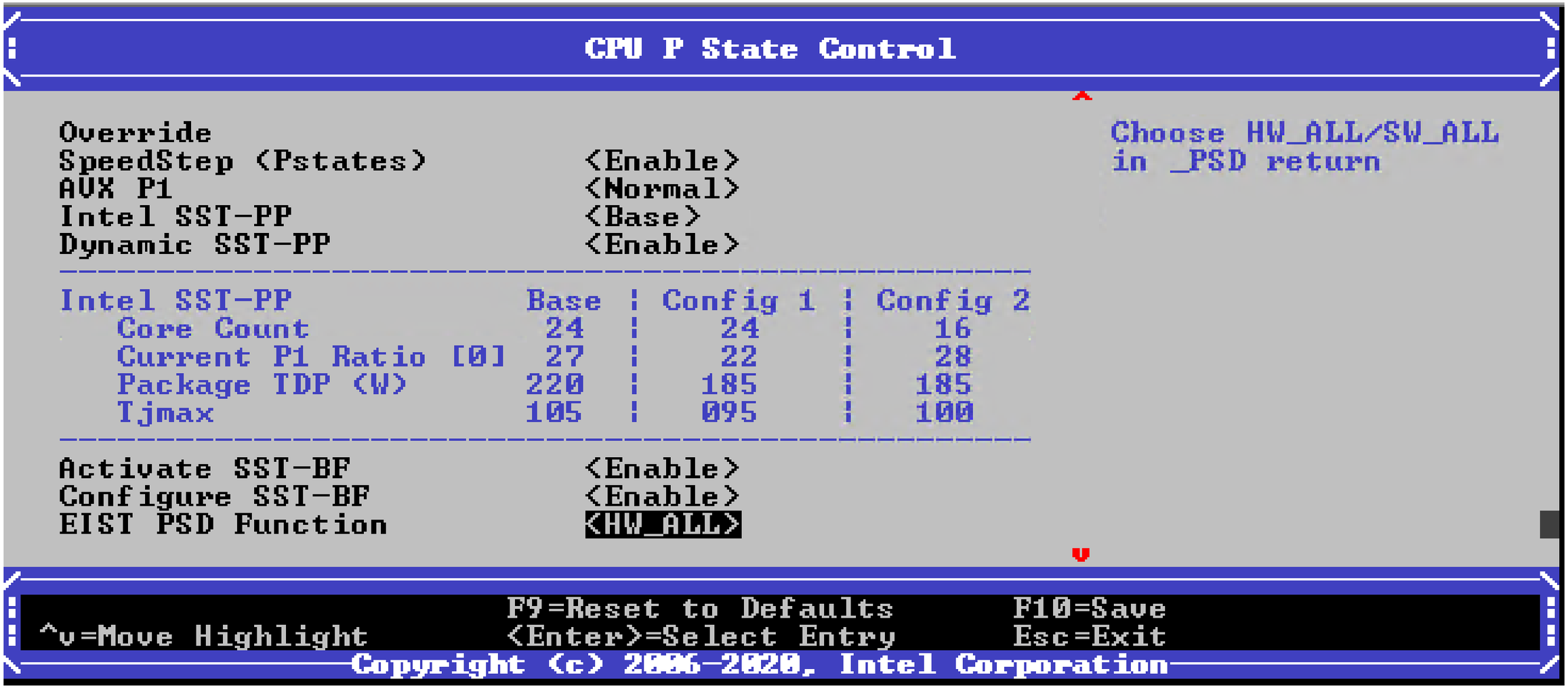
INTEL® SPEED SELECT TECHNOLOGY FEATURES: HOW TO

Intel® Speed Select Technology (Intel® SST) Features

Intel® SST-PP	Intel® SST-BF	Intel® SST-CP	Intel® SST-TF
Config 0	One set of HP/LP Cores and frequencies	Enable/Disable	Bucket 0 HP Core Count
			Bucket 1 HP Core Count
			Bucket 2 HP Core Count
Config 3	Not Available	Enable/Disable	Bucket 0 HP Core Count
			Bucket 1 HP Core Count
			Bucket 2 HP Core Count
Config 4	Not Available	Enable/Disable	Bucket 0 HP Core Count
			Bucket 1 HP Core Count
			Bucket 2 HP Core Count

Note: Specific Feature Availability and number of available configurations are SKU specific
Intel® Speed Select Technology–Performance Profile (Intel® SST-PP)
Intel® Speed Select Technology–Base Frequency (Intel® SST-BF)
Intel® Speed Select Technology–Core Power (Intel® SST-CP)
Intel® Speed Select Technology–Turbo Frequency (Intel® SST-TF)

BIOS setting screen



BIOS Setting: for all Intel® Speed Select Technology Features

Menu	Path to Setting		BIOS Setting	Required Setting
Socket Configuration	Advanced Power Management	CPU P-State Control	Intel® Advanced Vector Extensions (Intel® AVX) License Pre-Grant Override	Disable
			Enhance Intel Speed Step® Technology (P-States)	Enable
			Intel® SST-PP	Base
			Dynamic Intel® SST-PP	Enable
			Activate Intel® SST-BF	Enable
			Configure Intel® SST-BF	Enable
			EIST PSD Function	HW_ALL
			Boot Performance Mode	Maximum Performance
			Turbo Mode	Enable
		Hardware PM State Control	Hardware P-States	Native Mode with No Legacy Support
		Frequency Prioritization	Running Average Power Limit (RAPL) Prioritization	Enable
		CPU - Advanced PM Tuning → Energy Performance BIAS	Power Performance Tuning	BIOS Controls EPB
			Platform Environment Control Interface (PECI) Process Control System (PCS) Energy Bias Hint (EPB)	OS Controls EPB
			ENERGY_PERF_BIAS_CFG Mode	Performance

Intel® Speed Select Technology–Performance Profile

BIOS setting:

- Intel SST-PP = Base (this allow Intel SST-BF to functions)
- Intel SST-PP = Config1/Config2 (legacy) is equal to Config3/Config4

E.g. QU98

	Base	Config1 = Config3	Config1 = Config4
Active cores	24	24	16
P1 ratio	2.7GHz	2.2GHz	2.8GHz
TDP	220W	185W	185W

Intel® SST-PP represents Intel® Speed Select Technology–Performance Profile

Intel® Speed Select Technology–Performance Profile continued

Dynamic Intel® SST-PP: run time changes to Intel® SST-PP config level.

BIOS setting:

- Intel SST-PP = Base (this allow Intel SST-BF to functions)
- Dynamic SST-PP = Enable.

OS steps: Use intel-speed-select app to control SST-PP config level

- intel-speed-select perf-profile get-lock-status (return 0)
- intel-speed-select perf-profile set-config-level -l X –a (return success)
  - X = config level = 0,3,4
- intel-speed-select perf-profile get-config-current-level (return X)
- Refer to 621725_Intel-SST-for-Intel-Xeon-Processor_Compliance-Test-Guide-for-Linux_rev0p4: section 5.3.2 Intel® SST-PP: Functional for detail functional test instructions.

Intel® SST-PP represents Intel® Speed Select Technology–Performance Profile

Intel® Speed Select Technology–Base Frequency (Intel® SST-BF)

BIOS setting:

- Intel SST-PP = Base (this allow Intel SST-BF to functions)
- Activate SST-BF
- Configure SST-BF

	Base (SST-BF off)	Base (SST-BF on)
Active cores	24	8 HP cores + 16 LP cores
P1 ratio	2.7GHz	HP:2.9GHz + LP:2.5GHz
TDP	220W	220W

OS steps: SST-BF enabling and disabling can be done using “intel-speed-select” app:

- intel-speed-select base-freq enable
- Refer to 621725_Intel-SST-for-Intel-Xeon-Processor_Compliance-Test-Guide-for-Linux_rev0p4: section 5.3.6 Intel® SST-BF: Functional for detail functional test instructions.

Intel® Speed Select Technology–Core Power (Intel® SST-CP)

BIOS Setting:

- No specific Intel® SST-CP setting at BIOS menu.
- Frequency Prioritization -> Running Average Power Limit (RAPL) Prioritization -> Enable (This setting is a must for Intel® SST)

OS steps: “Intel-speed-select”

- intel-speed-select core-power enable (return success)
  - Clos = class of service
- First config a clos:-
  - intel-speed-select core-power config -c 0 -n X -m Y
  - Default all cores associated to clos_id = 0; X = clos min in MHz; Y = clos max in MHz
  - Refer to 621725_Intel-SST-for-Intel-Xeon-Processor_Compliance-Test-Guide-for-Linux_rev0p4: section 5.3.4 Intel® SST-CP: Functional for detail functional test instructions.

Intel® Speed Select Technology–Turbo Frequency (Intel® SST-TF)

BIOS Setting:

- No specific Intel® SST-CP setting at BIOS menu.
- Frequency Prioritization -> Running Average Power Limit (RAPL) Prioritization -> Enable (This setting is a must for Intel® SST)

OS steps: “Intel-speed-select”

- intel-speed-select turbo-freq enable (return success)
- intel-speed-select turbo-freq info –l 0 (return success)
- bucket 0,1,2’s high-priority core count e.g. bucket 0 = 4 cores, bucket 1 = 12 cores, bucket 2 = 20 cores
- Associate cpu core to clos_id:-
  - intel-speed-select --cpu 0-TOTAL CORES-1 core-power assoc -c 3 (make sure all call on low priority clos)
  - intel-speed-select --cpu 0-BUCKET0_MINUS_ONE core-power assoc -c 0 (make sure only bucket 0 count associate to high priority clos)
  - Refer to 621725_Intel-SST-for-Intel-Xeon-Processor_Compliance-Test-Guide-for-Linux_rev0p4: section 5.3.8 Intel® SST-TF: Functional for detail functional test instructions.

DOCUMENTATION

WW18'20 ICE LAKE HEATMAP (# 613226) UPDATES NOW AVAILABLE

Ice Lake Heatmap (#613226) Updates Now Available

- WW18’20 Ice Lake Heatmap (#613226) Updates Now Available on RDC

CEDAR ISLAND COOPER LAKE6 PINLIST – FINAL REVISION– RDC#601222 – R1.0

Cooper Lake-6 pins are locked and no more changes are planned. The current revision – 0.75 is being promoted to 1.0 on RDC.

Release of Cooper Lake-6 pinlist (RDC#601222) Rev 1.0

Whitley/Cedar Island Key Collateral Availability & Forecast

CPU Focus	Documents	Doc #	0.3	0.4	0.5	0.6	.65x	0.7	0.8	0.9x	1	1.5+	2
ICX	Ice Lake EDS v1	574451	Aug'17		Dec'17	Feb'18		Jan'19	WW09'20		May'20		
ICX	Ice Lake EDS v2	574942	Aug'17		Jan'18			Jan'19	WW10'20		May'20		
ICX	Ice Lake EDS v3	575291	Aug'17		Feb'18			Jan'19			**May'20**		
CPX-6UPI	Cooper Lake EDS v1	604785			Oct'18			WW34'19			**May'20**		
CPX-6UPI	Cooper Lake EDS v2(A, B)	604926 605073			Oct'18			Jul'19			Apr'20		
CPX-6UPI	Cooper Lake EDS v3	603686			Nov'18			WW35'19			**May'20**		
ICX	Socket P+ Pinlist	573771	Aug'17		Dec'17	Jan'18		Feb'18	July'18 Rev 0.9 New Pinout		Oct'18		
CPX-6UPI	CPX-6UPI Pinlist	601222			Oct'18			Nov'18			**Apr'20**		
All	Whitley PDG	574174	Aug'17		Nov'17	Feb'18	Aug'18 (WW35)	Oct'18	Dec'18 (WW51)	Rev 0.9 WW41'19	Q2'20		
CPX-6UPI	PDG Addendum	604036						Nov'18	WW06'19	Rev 0.9 Nov'19	Q2'20		
All	Whitley TMSDG	574080	Aug'17		Q1'18			Dec'18 (w/CPX)	May'19		Rev 1.01 Mar'20		
ICX	Ice Lake BWG	594768	Mar'18		Dec'18			Mar'2019			**Apr'20**		
CPX-6UPI	Cooper Lake BWG	607480	Dec'18		Feb'19			TBD			Mar'20		
ICX	Whitley RAS IVG	614168	Aug'19		Dec '19			Q2'20			**Q3'20**		
ICX	Wilson City RP	575544 (sch) 575545 (brd) 613040 (sch-SMT) 613039 (brd-SMT)			Dec'17		Aug'18 (WW34) New Pinout	Oct'18 (WW43)	Feb'19 (WW08'19)		Q4'19 Not Needed		
CPX-6UPI	Cooper City Modular RP	606823 (sch) 606817 (brd)	Dec'18					WW07'19	WW22'19		Not Needed		
ICX	Orion City PC	576577			Feb'18			Sept'18	WW06'19	WW28'19	WW43'19		
ICX	Tennessee Pass PC	613568			Combine w/ rev 0.7			Jun'19			Q2'20		
ICX	Coyote Pass PC	613661			Combine w/ rev 0.7			Jul'19			Q2'20		
CPX-6UPI	White Cloud City PC	610132 (sch) 610130 (brd)	Feb'19		Mar'19			May'19	WW40'19		Jan'20		
LBG/LBG-R	Lewisburg PCH EDS	547817											Rev 2.6 Aug'19 Rev 3.0 WW13'20
ICX	Heatmap	613226											
CPX6	Heatmap	618662											

Collaterals currently available Collaterals to be available in 2018 Collaterals to be available in 2019/2020 **RED BOLD TEXT**: updated info

LBG represents Lewisburg UPI represents Intel® Ultra Path Interconnect (Intel® UPI); ICX represents Ice Lake; CPX represents Cooper Lake

Full Collateral List

Collateral list

**Please be sure that you are signed in to access Technical Library content.

TOOLS AND DEBUG

DEBUG TOOLS ROADMAP UPDATE

Topics

- Key Points
- Tools Roadmaps by Segment
- Overview of Features vs. Solution
- Summary
- Debug Tools FAQs

Key Points in this Update

- Intel® System Debugger NDA (“White”) is now the debug solution for NDA customers. Intel® Platform Validation Toolkit “White” capabilities merged into Intel® System Debugger NDA as of WW45 2019
- Intel, Lauterbach* and Asset InterTech* supporting DbC
- Asset fully owns integration testing, validation and support of Intel® System Debugger NDA as necessary

These foils address a complex topic and all considerations may not be represented.

If you have questions, please engage your Intel representative before making a debug tools strategy decision.

Debug Tools Roadmap

Devices & Client

Empty	Not supported
✓	Internal Validation POR & avail. to OEMs.
O	Additional solutions for OEMs or internal.
#	ISD NDA (White) enabled, validated and supported by 3rd party

Intel probes from https://designintools.intel.com

Probe HW	Intel®			Lauterbach*			Asset*		
									
	ITP-XDP3BR	Closed Chassis Adapter (CCA)	DCI.DbC over USB T:Trace, X:DFx, D:DMA	DCI.DbC over USB	CombiProbe V2		Asset owns validation & support calls XDP3e	(BSSB)	over USB
					DCI OOB (BSSB)	MIPI60 (JTAG + MIPI PTI)			
Lakefield 1 Dev		✓	✓	O	O	O	#		#
Comet Lake Client	✓	✓	✓	O	O	O	#	#	#
Ice Lake Client, Rocket Lake		✓	✓	O	O	O	#	#	#
Tiger Lake Client	✓	✓	✓	O	O	O	#	#	#
Alder Lake Client		✓	✓	O	O		#		#
Elkhart Lake IOTG		✓	✓	O	O	O	#	#	#
Jasper Lake+	✓	✓	✓	O	O	O	#	#	#

Debug software from Intel (Intel® System Debugger NDA) can integrate with the Lauterbach* and Asset* transport solutions. Exception is the Lauterbach DCI.DbC transport solution which only works with Trace32.

ISS – Intel® System Studio
ISD – Intel® System Debugger - a component of Intel System Studio
PVT – Intel® Platform Validation Toolkit

Debug Tools Roadmap

uServer+

Empty	Not supported
✓	Internal Validation POR & avail. to OEMs.
O	Additional solutions for OEMs or internal.
#	ISD NDA (White) enabled, validated and supported by 3rd party
&	DCG or 3rd party distributed package of OpenIPC & ASD scripts

Intel probes from https://designintools.intel.com

	Intel®			Lauterbach*				Asset*			
											
Probe HW	**ITP-XDP3BR or BS2/3 for PPV**	**Closed Chassis Adapter** (CCA)	**DCI.DbC over USB** T:Trace, X:DFx, D:DMA	**DCI.DbC over USB**	**CombiProbe V2**		**QuadProbe**	**ECM-XDP3e**	**CCC (BSSB)**	**DCI.DbC over USB**	**At-Scale Debug**
					DCI OOB (BSSB)	**MIPI60** (JTAG + MIPI PTI)	**MIPI60** (JTAG + MIPI PTI)	**Asset owns validation & support calls**			
Ice Lake Server D	✓	✓	✓		O	O	O	#	#		&
Snow Ridge Server D	✓	✓	✓X		O	O	O				
Tanner Ridge Server D	✓	✓	✓X		O	O	O	#	#		&

Debug software from Intel (Intel® System Debugger NDA) can integrate with the Lauterbach* and Asset* transport solutions. Exception is the Lauterbach DCI.DbC transport solution which only works with Trace32.

ISS – Intel® System Studio
ISD – Intel® System Debugger - a component of Intel System Studio
PVT – Intel® Platform Validation Toolkit

Debug Tools Roadmap

Intel® Xeon® Server

Empty	Not supported
✓	Internal Validation POR & avail. to OEMs.
O	Additional solutions for OEMs or internal.
#	ISD NDA (White) enabled, validated and supported by 3rd party
&	DCG or 3rd party distributed package of OpenIPC & ASD scripts

Intel probes from https://designintools.intel.com

	Intel®				Lauterbach*				Asset*			
Probe HW	**ITP-XDP3BR or BS2/3 for PPV**	**Closed Chassis Adapter** (CCA)	**DCI.DbC over USB** T:Trace, X:DFx, D:DMA	**At-Scale Debug**	**DCI.DbC over USB**	**CombiProbe V2**		**QuadProbe**	**ECM-XDP3e**	**CCC (BSSB)**	**DCI. DbC over USB**	**At-Scale Debug**
						DCI OOB (BSSB)	**MIPI60** (JTAG + MIPI PTI)	**MIPI60** (JTAG + MIPI PTI)	**Asset owns validation & support calls**			
Cooper Lake, Cascade Lake AP	✓	✓	✓ T,D	&	O	O	O	O	#	#		&
Ice Lake Server SP	✓	✓	✓ T,D	&	O	O	O	O	#	#		&
Rocket Lake S Server	✓	✓	✓						#	#	#	
Ash Creek Falls	✓		✓			O	O	O				
Sapphire Rapids SP	✓	✓	✓	&	O	O	O	O	#	#	#	&

Debug software from Intel (Intel® System Debugger NDA) can integrate with the Lauterbach* and Asset* transport solutions. Exception is the Lauterbach DCI.DbC transport solution which only works with Trace32.

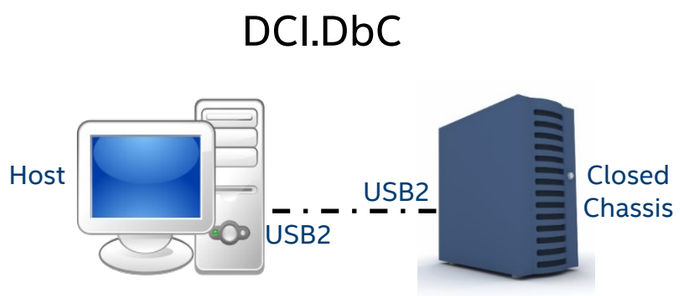
ISS – Intel® System Studio
ISD – Intel® System Debugger - a component of Intel System Studio
PVT – Intel® Platform Validation Toolkit

Overview of Features vs. Solution

Capability	Intel XDP3b "the blue box"	Intel Direct Connect Interface (DCI)	Intel® At Scale Debug BMC-JTAG *	Intel® At Scale Debug BMC-PECI	Lauterbach CombiProbe + PowerTrace	Lauterbach Combiprobe	Lauterbach QuadProbe + PowerTrace	Lauterbach Quadprobe	Lauterbach DbC	ASSET InterTech SourcePoint	ASSET InterTech ScanWorks Embedded Diagnostics
Common Usage Model	Power on, bench debug	Bench Debug	Deployed Debug	Autonomous & Interactive data collection	Power on, bench debug	Power on, bench debug	Power on, bench debug	Power on, bench debug	Bench debug	Power on, bench debug	Deployed Debug
Closed or Open Chassis	Open Chassis	Closed Chassis	Closed Chassis	Closed Chassis	Open Chassis	Open/Closed Chassis	Open Chassis	Open Chassis	Closed Chassis	Open/Closed Chassis	Closed Chassis
Adapter/Interface	XDP60**	USB2/BSSB	BMC	BMC	MIPI60	MIPI60 and BSSB	MIPI60	MIPI60	USB2	XDP60**, USB2 and BSSB	BMC
# Of Sockets	up to 8	up to 8	up to 8	up to 8	up to 8	up to 8	up to 32**	up to 32**	up to 8	up to 8	up to 8
Access Method	Local Host	Local Host	Remote Host	Remote Host	Local Host	Local Host	Local Host	Local Host	Local Host	Local Host	Remote Host
Source Level Debug	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Ask Asset
CPU Run Control & architectural debug	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PVT Integration	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes
CPU & PCH Register Access (Cscripts)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Error Injection (Cscripts)	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes
System Event Detection/Injection (reset, powergood, etc.)	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Red Cover Unlock with Intel Employee Present	Yes	Maybe/Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes
Red Cover Unlock PCH Early Break (halt PCH), Intel Employee present	Yes	No/Yes	No	No	Yes	Yes	Yes	Yes	No	Yes	No
DMA Write/Read into/out of Memory	No	Yes	No	No	No	No	No	No	Yes	No	No
System Tracing with Intel® Trace Hub	Yes	Yes	Yes*	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PTI Trace (Live Streaming)	No	No	No	No	Yes	Yes	Yes	No	No	No	No
HW Device Listed Price (US Dollars)	$900	$390	Reference Platform BOM	Reference Platform BOM	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact ASSET	Contact ASSET
SW Licensing Cost	PVT/ISS License	PVT/ISS License	PVT/ISS License	PVT/ISS License	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact Lauterbach	Contact ASSET	Contact ASSET

* Trace to memory. (Trace pins are not routed to BMC GPIOs per the white paper)
** For any designs above 8 sockets, contact an Intel FAE.
*** Reduced bandwidth. 1.6 Gbit/s on 8 bit port

Summary



- 14nm designs using OpenIPC in Intel® System Debugger for internal and external customers such as OxMs
- Intel System Debugger, a component of Intel® System Studio, is now the go to solution for system level debug. Intel® PVT “White” capabilities merged as of WW45’19 into Intel System Debugger NDA.
- ITP II (DAL) is in sustaining mode, no new features, Q3 2019
- Intel, Lauterbach and Asset InterTech supporting DbC

DAES Contacts

Tools Support

- Debugtoolssupport@intel.com
- http://goto/debugtoolssupport

Downloads

- http://goto.intel.com/downloadcenter
- Goto/pvt

IAGS/CPDP Contacts

Tools Support

- intelsystemstudio@intel.com

Downloads

- https://registrationcenter.intel.com/en/forms/?productid=2336

Debug Tools FAQs

1. Has Intel® In-Target Probe (Intel® ITP) PDT (DAL) software been EOL'd?

A: The Intel® ITP PDT (DAL) software product is feature complete and is in sustaining status as of Q3 2019. It continues to be available and supported for current customers on client and server programs as detailed in the Debug Tools Roadmap.

2. Can I still order Intel® ITP PDT (DAL) software?

A: Customers can continue to obtain licenses for Intel® ITP PDT (DAL) software through the Design-In Tools website (https://designintools.intel.com). Since there is not additional development planned after H1 2019, there is no longer a cost.

3. Is there a replacement software debug suite for the Intel® ITP PDT (DAL) software?

A: Yes, there are several options from multiple vendors, e.g. Intel (Intel® System Debugger), Asset InterTech* or Lauterbach*, which support multiple transport options including DCI DbC, DCI OOB, MIPI60 and legacy XDP60 as detailed in the Debug Tools Roadmap; goto/debugtoolsroadmap

Debug Tools FAQs continued

4. What is Intel® System Studio?

A: Intel® System Studio is a development tools suite that provides system debug & trace, system power/thermal & performance analysis, and build tools. The tools are intended for OxMs, SIs and other customers that are involved in system bring-up, platform enabling & validation, and general development of products based on Intel® Architecture.

5. What is Intel® System Debugger?

A: Intel® System Debugger, a component of Intel® System Studio, is ideal for platform bring-up and debugging of hardware, firmware, EFI/UEFI BIOS, operating systems, and device drivers. It allows debug of Windows* and Linux* kernel sources, and dynamically loaded drivers and kernel modules. Intel® System Debugger provides system debug & trace capabilities including a source level debugger, system trace based on Intel® Trace Hub, Crash Log analysis, Python* scripting, OS aware debugging, CScripts, and more. For Windows* target development it provides the Intel® Debug Extensions for WinDbg* which enables JTAG Debug & Trace for Microsoft* Windows* system, device driver and UEFI development. A developer can perform JTAG-based debug and trace over low-cost USB* connections or use a traditional JTAG probe.

Debug Tools FAQs continued

6. Is Intel® System Studio available for pre-launch products?

A: It is currently available to internal users and external customers with an Intel CNDA for several pre- launch products. Target date to expand this program to include all pre-launch IA products in Q2 2019.

7. How can customers get access to Intel® System Studio?

A: Please follow the **External NDA Customers** guideline for access to Intel® System Studio NDA. External **non-NDA** customers can learn more about the product at link

8. Has the Intel® ITP XDP hardware been EOL'd?

A: No. There are no plans to EOL the Intel® ITP XDP hardware.

Debug Tools FAQs continued

9. Is a hardware probe still required?

A: The hardware requirements for each solution are described in the Debug Tools Roadmap foils above

10. How do I obtain any of the hardware transports, e.g. probes?

A: Intel products and pricing are available at the Design-In Tools store located at https://designintools.intel.com/

A: Lauterbach information and products are available at: www.lauterbach.com/frames.html?home.html

A: Asset InterTech product and pricing information is available at: www.asset-intertech.com/

INTEGRATED CHANNEL ANALYSIS TOOL (ICAT) 4.200.15 AVAILABLE

ICAT 4.200.15 Available

The *Integrated Channel Analysis Tool (ICAT)*, version 4.200.15, document #626177, has been released.

This version adds a number of new features, including

- Independent surface roughness controls in the Channel Builder field solver.
- Improved empirical (bitstream) extrapolation and sampling routines
- IBIS 7.0 AMI Rx Noise parameters are recognized and accepted.
- DDR DFE sweep and override controls, including disable, are now available.

In addition, several bug fixes related to crashes have been addressed.

See the release notes for complete details.

WHITLEY TOOLS UPDATE

5/5/2020 0.13

WHITLEY TOOL READINESS

Advanced Debug Tools Methodology (ADTM)

May 5, 2020-Rev 0.13

Whitley Tools Readiness

- **NOTE: OEMs must enable in BIOS- PcdBiosDfxKnobEnabled|TRUE for the tools to properly work.**
- Ice Lake I/O Margin Tool*
  - **Customers and BIOS vendors need to enable EV DFx Features in BIOS Setup – all knobs documented in User Guide should be accessible**
- Ice Lake XCC C0 support in Ice Lake CScripts v1.01 ww14
- Ice Lake CScripts v1.02 available in RDC
  - Bug Fixes and Features
    - Memory: Issues with memory topology and address translation
    - Error Injection: Introduce Patrol Scrub injection
    - PCI Express: Remove all LTSSM lt_loop memory leaks
    - More information can be found on Release Notes
- Redfish support in Ice Lake CScripts v1.1 ww24
  - 3 weeks due to Cooper Lake delays plus 2 weeks delay due to queue backlog for RDC posting.
- **For CScripts please use ISS/ISD NDA 2014:** registrationcenter
  - How to obtain Intel® System Debugger NDA: 135409.547119.105695
- ISS/ISD Public Documents
  - introducing-the-intel-system-debugger
  - get-started-with-system-debug
  - system-debug-user-guide
  - get-started-with-socwatch

RDC/KIT#	Tool Name	Target*	Trending
572261	Ice Lake CScripts (1.0)	Now	N/A
576860	DTC Error Injection	Now	N/A
615113	ICAT	Now	N/A
MM 999KVK	IDV aka MiTiBug	Now	N/A
134322	Intel® Platform Validation Toolkit (Intel® PVT) Intel® At-Scale Debug (Intel® ASD)	Now	N/A
524152	Intel® SelfTest	Now	N/A
135408-Win 135409-Linux	Intel® System Studio/ Intel® System Debugger	Now	N/A
616405	Intel® C620 Series Chipset Intel® IO Margin Tool		
613291 611947-Base 603471-UG	Ice Lake Intel® IO Margin Tool Ice Lake Base Platform Server Testing Intel® I/O Margin Tool Ice Lake UG	Now	N/A
MM 940990 lauterbach x86	Intel® In-Target Probe /XDP3B & Lauterbach	Now	N/A
564141	MEI Test Card (DDR4 Only)	Now	N/A
613249	MKTME Checker	Now	N/A
610667 MM PCIERRINJ	PEI Gen4 Test Card	Now	N/A
611974	Intel® Platform Firmware Resilience (Intel® PFR) Provisioning Tool	Now	N/A
615179-WIN 615178-LNX	Intel® Power Thermal Utility (Intel® PTU) (Windows* & Linux*), 615177 -User Guide	Now	N/A
611498	RMT and Intel MMA	Now	N/A
575969 132857-Model 133027-Lib Spprt	SIMICS	Now	N/A
registrationcenter	Intel SoC Watch	Now	N/A
Intel Rep	Thermal Test Vehicle (TTV)	Now	N/A
563989	TPM Provisioning	Now	N/A
612919	Intel® Trusted Execution Technology (Intel® TXT) Toolkit	Now	N/A
612282 MM 960764	VRTT	Now	N/A

SRMT (State Residency and Management Tool)

Effective immediately SRMT is EOL. Intel® SoC Watch will replace SRMT.

NOTE: SoC Watch is a passive (monitor) tool.

1. Customer must used iLVSS (intel Linux Validation Stress Suite) 564312 or iWLVSS (intel Window Validation Stress Suite) 564311 for platform stress. Please contact Intel representative for access.

2. SoC Watch test document 626226

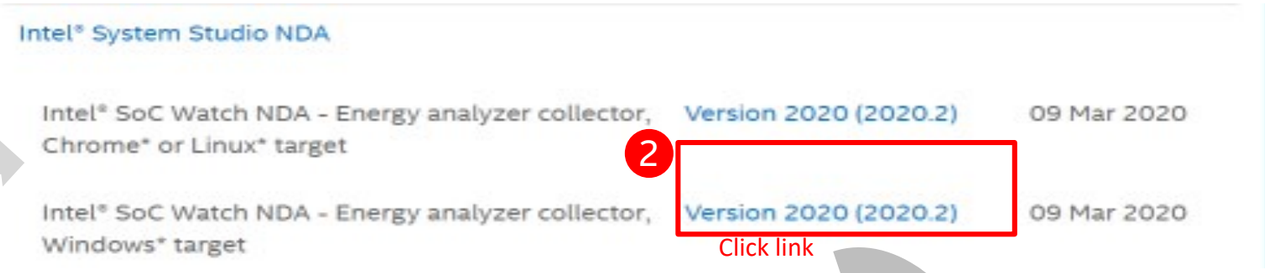
1, 2, 3 steps to get Intel® SoC Watch NDA

1) **Fill-in online form** to request Intel® System Studio NDA. Wait for the notification email with download instructions.

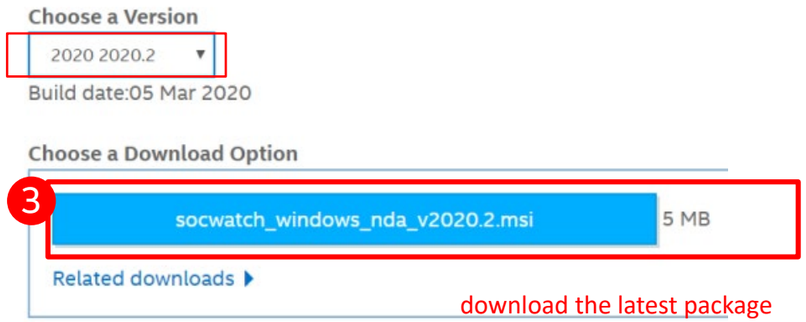
1

link: https://registrationcenter.intel.com/en/forms/?productid=2336&SupportCode=ENA

2) **Login** *registrationcenter.intel.com/en/products/* with VIP/IBL/IDZ/... account (if you do not have any account, **create one** today!)



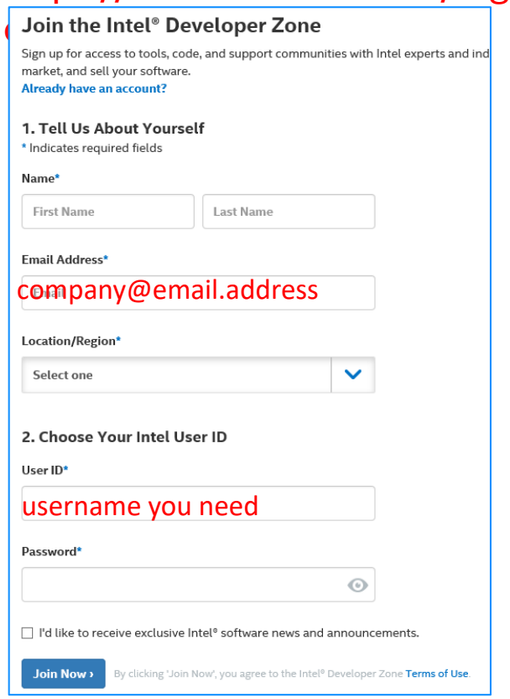
3) **Download** the **latest** Intel® SoC Watch NDA



Fill-in online form

create one account today!

https://software.intel.com/registrati



INTEGRATED CHANNEL ANALYSIS TOOL (ICAT) 4.200.15 AVAILABLE

ICAT 4.200.15 Available

The *Integrated Channel Analysis Tool (ICAT)*, version 4.200.15, document #626177, has been released.

This version adds a number of new features, including

- Independent surface roughness controls in the Channel Builder field solver.
- Improved empirical (bitstream) extrapolation and sampling routines
- IBIS 7.0 AMI Rx Noise parameters are recognized and accepted.
- DDR DFE sweep and override controls, including disable, are now available.

In addition, several bug fixes related to crashes have been addressed.

See the release notes for complete details.

I/O MARGIN TOOL RELEASE CLARIFICATION FOR ICE LAKE PLATFORMS

I/O Margin Tool Release Clarification for Ice Lake/Cooper Lake Platforms

Platform	Silicon	I/O Margin Tool Distribution / Revision / Doc#	Installer	Access Mode Support		Interface Support					Note
				Host-Based	On-Target	UPI	UPI TxEq	CPU PCIe	CPU DMI	PCH	
Whitley (Ice Lake HCC/XCC)	ICX	Ice Lake-I/O Margin Tool v3.0 (Doc# 613291)	Ice Lake IPSS Installer Win64-3.0.3.exe	v	v	v	v	v	v	x	Python 3.6 based ISD/ISS NDA-2010
Whitley/Cedar Island	LBG	LBG I/O Margin Tool v1.3 (Doc# 616405)	LBG IPSS Installer Win64-1.3.0.013.exe	v	V	x	x	x	x	v	Python 2.7 based ISD/ISS NDA-1949

Notes:

- v indicates support, x indicates no support
- For target system incorporating Ice Lake LCC, I/O Margin Tool 2.1 is applicable for both CPU and PCH
- Ice Lake I/O Margin Tool 3.0 release incorporates XCC support, Python3.6 environment and bug fixes
- Refer to I/O Margin Tool release note for information about recommended OpenIPC software (Intel System Debugger, aka ISD) version to be used with I/O Margin Tool

Platform	Silicon	I/O Margin Tool Distribution / Revision / Doc#	Installer	Access Mode Support		Interface Support					Note
				Host-Based	On-Target	UPI	UPI TxEq	CPU PCIe	CPU DMI	PCH	
Cedar Island	Cooper Lake-6	Cooper Lake-6 I/O Margin Tool v2.0.05 (Doc# 616404)	Cooper Lake IPSS Installer Win64-2.0.05.exe	v	V	v	v	v	v	x	Python 3.6 based ISD/ISS NDA-1949
Whitley/Cedar Island	LBG	LBG I/O Margin Tool v1.3 (Doc# 616405)	LBG IPSS Installer Win64-1.3.0.013.exe	v	V	x	x	x	x	v	Python 2.7 based ISD/ISS NDA-1949

Notes:

- v indicates support, x indicates no support
- LBG IOMT fail detection for LBG-QDF numbers, it's already fixed in 1.3 installer
- Refer to I/O Margin Tool release note for information about recommended OpenIPC software (Intel System Debugger, aka ISD) version to be used with I/O Margin Tool

Whitley Tool Readiness continued

I/O Margin Tool continued

- If EV DFX is not enabled, an error message will be recorded in a self-generated log file. Example:

```
try and remove file C:\Intel\IPSS\ipss1.0\Lib\site-packages\evToolsTests\localTestsRepository\iomargin\results\CPU-
UPI\Results_20190801_110331639\20190801_114337_974000.tsv  General Normal  Information    08/01/2019     11:48:04
Margin is complete    Public  Normal  Information    08/01/2019     11:48:04
errorDict.keys() = None, marginCompleted = True     General Normal  Information    08/01/2019     11:48:04
Error: Traceback (most recent call last):    Public  Normal  Information    08/01/2019     11:48:04
File "C:\Intel\IPSS\ipss1.0\lib\site-packages\evContent\base\base.py", line 531, in resultSummarize     Public  Normal
       Information    08/01/2019     11:48:04
return status, newResultFile  Public  Normal  Information    08/01/2019     11:48:04
UnboundLocalError: local variable 'newResultFile' referenced before assignment    Public  Normal  Information    08/01/2019
       11:48:04
Error: Traceback (most recent call last):    Public  Normal  Information    08/01/2019     11:48:04
File "C:\Intel\IPSS\ipss1.0\lib\site-packages\evContent\base\base.py", line 336, in runMargin    Public  Normal  Information
       08/01/2019     11:48:04
status, filename = self.resultSummarize(marginData, context, requestId)    Public  Normal  Information    08/01/2019     11:48:04
TypeError: 'int' object is not iterable      Public  Normal  Information    08/01/2019     11:48:04
```

Can use c-script to double check if EV DFX is enabled or not. See next page

Checking for DFX enable for Intel® IO Margin Tool

Use the following command line in Whitley CScripts to verify whether or not EV DFX is enabled in the BIOS of a SUT (System Under Test)

```
>>> sv.socket0.uncore.pcie.pxps.port0.msg.acwrpr6
```

Examples:

EV DFX enabled:

```
>>> sv.socket0.uncore.pcie.pxps.port0.msg.acwrpr6
socket0.uncore.pcie.pxp0.port0.msg.acwrpr6 - [96b] 0x000000002000040003000021B
socket0.uncore.pcie.pxp1.port0.msg.acwrpr6 - [96b] 0x000000002000040003000021B
socket0.uncore.pcie.pxp2.port0.msg.acwrpr6 - [96b] 0x000000002000040003000021B
socket0.uncore.pcie.pxp3.port0.msg.acwrpr6 - [96b] 0x000000002000040003000021B
```

EV DFX Disabled:

```
>>> sv.socket0.uncore.pcie.pxps.port0.msg.acwrpr6
socket0.uncore.pcie.pxp0.port0.msg.acwrpr6 - [96b] 0x000000002000040001000020A
socket0.uncore.pcie.pxp1.port0.msg.acwrpr6 - [96b] 0x000000002000040001000020A
socket0.uncore.pcie.pxp2.port0.msg.acwrpr6 - [96b] 0x000000002000040001000020A
socket0.uncore.pcie.pxp3.port0.msg.acwrpr6 - [96b] 0x000000002000040001000020A
```

Whitley Tool Readiness continued

Intel® Platform Validation Toolkit (Intel® PVT) with Intel® At-Scale Debug (Intel® ASD) is available in VIP portal

- Starting ww01'20 the Intel® PVT (standalone w/o Intel® ASD) is no longer available in VIP portal. Intel® PVT is integrated into ISS/ISD Tool. Note: PVT in ISS/ISD does not support Intel® ASD Intel® System Studio/Intel® System Debugger update information
- How to obtain Intel® System Debugger NDA: registrationcenter-New User
- Link to the Intel System Debugger NDA overview presentation: Intel System Debugger 2019 NDA_1945 30-3-30
- Intel System Studio/ Intel System Debugger 2019 NDA 1949 and prior releases supports Python* 2.x and Python 3.x.
- U2010 version is the last version of the Intel System Debugger to be posted in VIP. After that this tool will only be posted in Intel Registration center
  - First time user must follow the pdf on "How to obtain Intel System Debugger NDA"
  - Repeated user will login to IRC link registrationcenter

CEDAR ISLAND TOOLS UPDATE

5/5/2020-0.12

CEDAR ISLAND TOOL READINESS

Advanced Debug Tools Methodology (ADTM)

May 5, 2020-0.12

Cedar Island Tools Readiness

- **NOTE: OEMs must enable in BIOS- PcdBiosDfxKnobEnabled|TRUE for the tools to properly work.**
- CScripts
  - Cooper Lake6 CScripts v1.0 ww18 with IPMI, Redfish and QS support
  - Note: 614082 supports Cooper Lake6
  - **Please use ISS/ISD NDA 2014: registrationcenter**
    - How to obtain Intel® System Debugger NDA: 135409.547119.105695
- ISS/ISD Public Documents
  - introducing-the-intel-system-debugger
  - get-started-with-system-debug
  - system-debug-user-guide

RDC/Kit#	Tool Name	Target*	Trending
614082	Cooper Lake-6 CScripts (0.99)	Now	N/A
576860	DDR4 DTC Error Injection	Now	N/A
615113	ICAT	Now	N/A
MM 999KVK	*IDV aka MiTiBug	Now	N/A
134322	Intel® Platform Validation Toolkit (Intel® PVT) Intel® At-Scale Debug (Intel® ASD)	Now	N/A
524152	Intel® SelfTest	Now	N/A
619731-Win 611551-Linux	Intel® System Studio/Intel® System Debugger	Now	N/A
616405	LBG I/O Margin Tool	Now	N/A
616404	Cooper Lake-6 I/O Margin tool	Now	N/A
MM 940990 lauterbach x86	Intel® In-Target Probe/XDP3B & Lauterbach	Now	N/A
564141	MEI Test Card (DDR4 Only)	Now	N/A
611974	PFR Provisioning Tool	Now	N/A
615179-Win 615178-Lnx 615177-UG	Intel® Power Thermal Utility (Intel® PTU) (Windows* & Linux*), User Guide	Now	N/A
616436 616250	RMT and Intel® Memory Margin Analyzer (Intel® MMA)	Now	N/A
575969 132857-Model 133027-Lib Spprt	SIMICS	Now	N/A
registrationcent	Intel SoC Watch	Now	N/A
Intel Rep	Thermal Test Vehicle (TTV)	Now	N/A
563989	TPM Provisioning	Now	N/A
612919	Intel® Trusted Execution Technology (Intel® TXT) Toolkit	Now	N/A
612282 MM 960764	VRTT	Now	N/A

SRMT (State Residency and Management Tool)

Effective immediately SRMT is EOL. Intel® SoC Watch will replace SRMT.

NOTE: SoC Watch is a passive (monitor) tool.

1. Customer must use Intel® Validation Stress Suite – Linux*, 564312 or Intel® Validation Stress Suite – Window* 564311 for platform stress.
2. SoC Watch test document 626226 ww19.4.

SRMT (State Residency and Management Tool)

Effective immediately SRMT is EOL. Intel® SoC Watch will replace SRMT.

NOTE: SoC Watch is a passive (monitor) tool.

1. Customer must used iLVSS (intel Linux Validation Stress Suite) 564312 or iWLVSS (intel Window Validation Stress Suite) 564311 for platform stress. Please contact Intel representative for access.

2. SoC Watch test document 626226

1, 2, 3 steps to get Intel® SoC Watch NDA

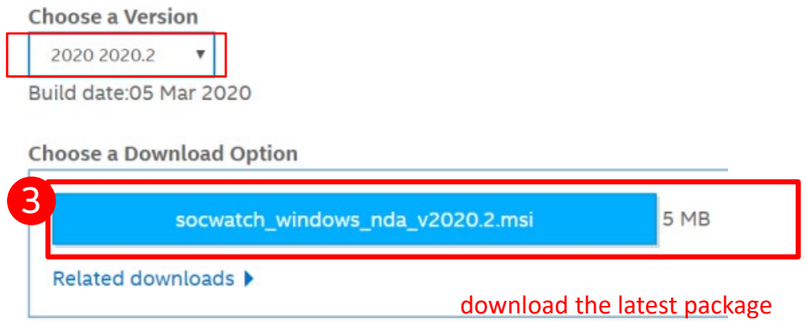
1) **Fill-in online form** to request Intel® System Studio NDA. Wait for the notification email with download instructions.

1

link: https://registrationcenter.intel.com/en/forms/?productid=2336&SupportCode=ENA

2) **Login** *registrationcenter.intel.com/en/products/* with VIP/IBL/IDZ/... account (if you do not have any account, **create one** today!)

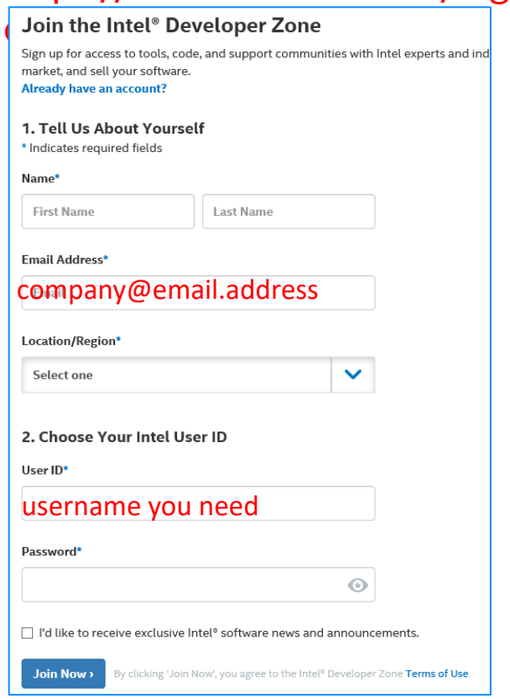
3) **Download** the **latest** Intel® SoC Watch NDA



Fill-in online form

create one account today!

https://software.intel.com/registrati



I/O MARGIN TOOL RELEASE CLARIFICATION FOR ICE LAKE / COOPER LAKE PLATFORMS

Intel® IO Margin Tool Release Clarification for Ice Lake/Cooper Lake Platforms

Platform	Silicon	I/O Margin Tool Distribution / Revision / Doc#	Installer	Access Mode Support		Interface Support					Note
				Host-Based	On-Target	UPI	UPI TxEq	CPU PCIe	CPU DMI	PCH	
Whitley (Ice Lake HCC/XCC)	ICX	Ice Lake-I/O Margin Tool v3.0 (Doc# 613291)	Ice Lake IPSS Installer Win64-3.0.3.exe	v	v	v	v	v	v	x	Python 3.6 based ISD/ISS NDA-2010
Whitley/Cedar Island	LBG	LBG I/O Margin Tool v1.3 (Doc# 616405)	LBG IPSS Installer Win64-1.3.0.013.exe	v	V	x	x	x	x	v	Python 2.7 based ISD/ISS NDA-1949

Notes:
- v indicates support, x indicates no support
- For target system incorporating Ice Lake LCC, I/O Margin Tool 2.1 is applicable for both CPU and PCH
- Ice Lake I/O Margin Tool 3.0 release incorporates XCC support, Python3.6 environment and bug fixes
- Refer to I/O Margin Tool release note for information about recommended OpenIPC software (Intel System Debugger, aka ISD) version to be used with I/O Margin Tool

Platform	Silicon	I/O Margin Tool Distribution / Revision / Doc#	Installer	Access Mode Support		Interface Support					Note
				Host-Based	On-Target	UPI	UPI TxEq	CPU PCIe	CPU DMI	PCH	
Cedar Island	Cooper Lake-6	Cooper Lake-6 I/O Margin Tool v2.0.05 (Doc# 616404)	Cooper Lake IPSS Installer Win64-2.0.05.exe	v	V	v	v	v	v	x	Python 3.6 based ISD/ISS NDA-1949
Whitley/Cedar Island	LBG	LBG I/O Margin Tool v1.3 (Doc# 616405)	LBG IPSS Installer Win64-1.3.0.013.exe	v	V	x	x	x	x	v	Python 2.7 based ISD/ISS NDA-1949

Notes:
- v indicates support, x indicates no support
- LBG IOMT fail detection for LBG-QDF numbers, it's already fixed in 1.3 installer
- Refer to I/O Margin Tool release note for information about recommended OpenIPC software (Intel System Debugger, aka ISD) version to be used with I/O Margin Tool

Cedar Island Tool Readiness continued

Intel® Platform Validation Toolkit (Intel® PVT) with Intel® At-Scale Debug (Intel® ASD) is available in VIP portal

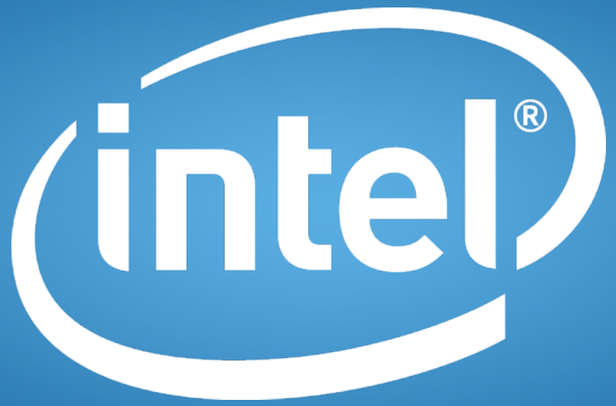
- Starting ww01'20 the Intel® PVT (standalone w/o Intel® ASD) is no longer available in VIP portal. PVT is integrated into Intel® System Studio /Intel® System Debugger Tool. Note: Intel® PVT in Intel® System Studio/Intel® System Debugger does not support ASD (At-Scale Debug)

Intel System Studio/Intel System Debugger update information

- How to obtain Intel® System Debugger NDA: registrationcenter-New User
- Link to the Intel System Debugger NDA overview presentation: Intel System Debugger 2019 NDA_1945 30-3-30
- Intel System Studio/ Intel System Debugger 2019 NDA 1949 and prior releases supports Python 2.x and Python 3.x.
- U2010 version is the last version of the Intel System Debugger to be posted in VIP. After that this tool will only be posted in Intel Registration center
  - First time user must follow the pdf on "How to obtain Intel System Debugger NDA"
  - Repeated user will login to IRC link registrationcenter

OEM COMMUNICATIONS AND FEEDBACK

SOFTWARE


intel