



Kaby Lake PCH Initialization Code Version 3.8.0

Release Notes

April 2020

Revision 3.8.0

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1 Introduction

- Product: Kaby Lake PCH Initialization Code
- Developed by: Intel Corporation
- Software version released date: <April/2020>

Note: This document is cumulative and includes information on previous versions. The version information is presented with the newest release first and then regressing through earlier versions.

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Note: Visual Studio 2013 Update 5 patch is needed.

Update with release information can be obtained at following link:

<https://support.microsoft.com/en-in/help/3021976/description-of-visual-studio-2013-update-5>

1.1 Purpose of Initialization Code

This is sample Initialization Code for Kaby Lake PCH. It is used to initialize and control the Intel PCH modules in the system pre-boot process. It complies with Kaby Lake PCH BIOS specification for all programming requirements.

1.2 Target Customers

The Kaby Lake PCH Initialization Code is intended for use as part of Intel BIOS. The code is compatible with both mobile and desktop products.



1.3 Version Release History

Version	Description	Release Date
0.5.0.0	Initial release	December 3, 2015
0.6.0.0	Alpha Y/U	January 7, 2016
0.6.1.0	Alpha Y/U Update	January 29, 2016
0.7.0.0	Beta Y/U	February 16, 2016
0.7.1.0	Beta Y/U Update	March 09, 2016
0.7.2.0	Beta Y/U Update	March 24, 2016
0.7.3.0	U/Y Beta Update DT with SPT Alpha Cons/Corp Halo Alpha Cons/Corp	April 4, 2016
0.8.0.0	U/Y Beta Update	April 12, 2016
0.8.1.0	U/Y Beta Update	May 9, 2016
0.9.0.0	<ul style="list-style-type: none">• U/Y PC candidate• DT with SPT Alpha Cons/Corp update• Halo Alpha Cons/Corp update	May 18, 2016
0.9.1.0	<ul style="list-style-type: none">• U/Y Production candidate• DT with SPT Alpha Cons/Corp update• Halo Alpha Cons/Corp update	June 02, 2016
1.0.0.0	<ul style="list-style-type: none">• U/Y HR'16 RS1• U23e Alpha SR'17 S/H/Y/U Beta	June 08, 2016
1.0.1.0	<ul style="list-style-type: none">• U/Y HR'16 RS1• U23e Alpha RS1 SR'17 S/H/Y/U Beta	June 17, 2016
1.0.2.0	SR'17 U/Y/S/H Beta	June 30, 2016
1.0.3.0	SR'17 U/Y/S/H RS1 Beta update	July 15, 2016
1.0.4.0	Update copyright heard/no other change	August 12, 2016
1.0.5.0	Update U/Y HR'16 RS1, SR'17 U/Y/S/H Update, Update U23e Alpha RS1	August 31, 2016
1.1.0.0	PV U/Y HR'16 RS1, SR'17 U/Y/S/H Update, Update U23e Alpha RS1	September 21, 2016
1.2.0.0	PV SR'17 S42 – consumer PCV SR'17 Y/U Update PCV SR'17 H/U32e/ all Corp SKUs	October 07, 2016
1.3.0	No change	October 20, 2016
1.4.0	PV SKL on KBL platform with Win 7/8.1 SR'17 – PR1 Update U32e	November 4, 2016
1.4.1	Optane enabling update only	November 20, 2016



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1.5.0	PV SKL on KBL Platforms with Win7/Win8.1 Post SR'17 update – PR2 Update to U23e	December 1, 2016
1.6.0	Post SR'17 update for PR2	December 19, 2016
1.7.0	Pre-ES KBL-R Post SR'17 update	February 06, 2017
1.8.0	KBL-R support Post SR'17 update	February 22, 2017
1.9.0	KBL-R Pre-Beta support Post SR'17 update	March 09, 2017
2.0.0	KBL-R Beta support Post SR'17 update	March 22, 2017
2.1.0	KBL-R Beta support Post SR'17 update	April 04, 2017
2.2.0	KBL-R update Post SR'17 update	April 25, 2017
2.3.0	Added Coffee Lake-S support	May 19, 2017
2.2.1	KBL-R PC/PV RS2 PC/PV See note about this release vs 2.3.0 in version details	May 25, 2017
2.4.0	KBL-R PC/PV RS2 PC/PV CFL-S with Kaby Point PCH Beta Combined 2.2.1 and 2.3.0 release, See note about 2.2.1 release vs 2.3.0 release in version details	June 01, 2017
2.5.0	Pre-ES KBL-R Post SR'17 update	June 22, 2017
2.5.1	KBL/PV KBL-R/ PV CFL-S with Kaby Point PCH Beta Aligning with KBL/KBL-R RS2 corporate PV BKC Release.	July 6, 2017
2.6.0	KBL/PV KBL-R/ PV CFL-S with Kaby Point PCH Beta Aligning with CFL-S with Kaby Point PCH BKC Release .	July 19, 2017
2.6.1	KBL/PV KBL-R/ PV CFL-S with Kaby Point PCH Beta Aligning with CFL-S with Kaby Point PCH BKC Release .	August 2, 2017



2.6.2	KBL/PV KBL-R/ PV CFL-S with Kaby Point PCH PV Aligning with CFL-S with Kaby Point PCH RS2 PV BKC Release .	August 9, 2017
2.7.0	KBL/KBL-R RS3 WW33 BKC CFL-S with Kaby Point PCH Aligning with KBL/KBL-R BKC release WW33 RS3	August 15, 2017
2.7.2	KBL/KBL-R RS3 WW36 BKC RS3 CFL-S with Kaby Point PCH PR1 RS2 Aligning with KBL/KBL-R BKC WW36 RS3 & CFL S 62 /CFL S 42 + KBP-H PCH PR1 RS2	September 7, 2017
2.8.0	KBL/KBL-R RS3 WW39 BKC Aligning with KBL/KBL-R BKC WW39 RS3	September 27, 2017
2.8.1	KBL/KBL-R RS3 WW41 BKC Aligning with KBL/KBL-R BKC WW41 RS3	October 13, 2017
2.9.0	KBL/KBL-R RS3 WW44 BKC Aligning with KBL/KBL-R BKC WW41 RS3	October 31, 2017
2.9.2.0	CFL-S with Kaby Point PCH Aligning with CFL-S62/S42 + KBP-H BKC WW47 RS3	November 2017
3.0.0.0	KBL/PV KBL-R/ PV Aligning with KBL legacy U22/S42/H42 PV BKC release WW49	December 2017
3.0.1.0	KBL-R update	December 2017
3.1.1.0	CFL-S with Kaby Point PCH Aligning with CFL-S62/S42 + KBP-H Consumer PV BKC WW06 RS3 BKC	February 9, 2018
3.1.2.0	CFL-S with Kaby Point PCH Aligning with CFL-S62/S42 + KBP-H Consumer PR1 BKC WW10 RS3	March 5, 2018
3.2.0	KBL-R update	April 11, 2018
3.2.1	KBL-Y Refresh update	May 10, 2018
3.3.0	KBL-Y Refresh update	May 18, 2018
3.3.1	Aligning with KBL/KBL-R RS4 Beta BKC	June 21, 2018
3.4.0	Aligning with AML-Y22 5W PV BKC	June 21, 2018
3.5.0	CFL S82 with Kaby Point PCH Aligning with Coffee Lake S82, KBP-H Beta BKC RS3 WW25	June 21, 2018
3.6.0	KBL-G RS4 Corp BKC release WW26'2018	June 29, 2018
3.6.1	Aligning with AML-Y22 5W PR1 BKC WW29'2018	July 20, 2018
3.6.1.1	Aligning with KBL-R RS4 PV BKC WW32.1'2018	August 1, 2018
3.6.2	Aligning with AML-Y22 7W PV BKC WW31'2018	August 2, 2018
3.6.3	Aligning with CFL S82, Kaby lake PCH-H PV BKC RS4 WW37'2018	September 14, 2018



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3.6.4	Aligning with AML Y22 5W RS5 Beta WW40'2018	October 4, 2018
3.6.5	Aligning with RS5 WW43'2018	October 22, 2018
3.6.6	Aligning with WW46' 2018	November 14, 2018
3.6.7	Aligning with WW47' 2018	November 16, 2018
3.6.7.1	Aligning with KBL-U42 RS5 PV BKC WW51'2018	December 16, 2018
3.6.8	Aligning with KBL-U42 RS5 PV BKC WW52'2018	December 26, 2018
3.6.9	Aligning with AML Y42 RS5 Beta BKC WW03'2019	January 14, 2019
3.7.0	Update for KBL/KBL-R/AML	March 6, 2019
3.7.1	Update for KBL/KBL-R/AML	March 29, 2019
3.7.2	Aligning with Coffee Lake S82/62/42 Kaby Lake PCH-H Consumer Beta BKC 19H1 WW17'2019	April 24, 2019
3.7.3	Aligning with AML Y42/Y22 QS BKC 19H1 WW18'2019	May 06, 2019
3.7.4	Update for KBL/KBL-R/AML Aligning with AML Y42/Y22 PV BKC 19H1 WW23'2019	June 04, 2019
3.7.5	Aligning for Coffee Lake S82/62/42 Kaby Lake PCH-H Consumer Production Version (PV) BKC 19H1 WW23'2019	Jun 10, 2019
3.7.6	Update for KBL/KBL-R/AML	September 1, 2019
3.7.7	Aligning for AML Y42 Best Known Configuration (BKC) Software Package (WCOS 20H1) WW51'2019	December 22, 2019
3.7.8	Update for KBL-YR/KBL-R/KBL/AML .	Jan 16, 2020
3.7.9	Update for KBL-YR/KBL-R/KBL/AML .	March 03, 2020
3.8.0	Update for KBL-R/KBL/CFL	April 01, 2020



2 Version 3.8.0 Details

2.1 New Features

- None

2.2 Fixed Bugs

- None



3 Version 3.7.9 Details

3.1 New Features

3.1.1 Feature 1

- **Description:**
 - Added Touch Panel ACPI code + NVS Variables + Setup menus
 - Added presets for ELAN and WACOM
 - Added option of configuring Custom Touch Panel
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl

3.2 Fixed Bugs

3.2.1 Bug 1

- **Description:**
Can't recognize the USB 3.0 add-on card in PCIe slot3
- **Solution:**
Adjusted defaults
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiDxeSmmRstPrivateLib/PeiDxeSmmRstPrivateLib.c



4 Version 3.7.8 Details

4.1 New Features

4.1.1 Feature 1

- **Description:**
Add support for a new KBL-H SKUs
- **Solution:**
Add support for a new KBL-H SKUs two new skus
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

4.1.2 Feature 2

- **Description:**
Add Sound Research support
- **Solution:**
Added new 3rd party IP support: Sound Research IP
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakePlatSamplePkg/Setup/PchSetup.hfr
/KabylakePlatSamplePkg/Setup/PchSetup.uni
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h

4.1.3 Feature 3

- **Description:**
New Kabylake Family ID Changes for CPU
- **Solution:**
KBL Code Changes to handle new KBL Family IDs
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakePlatSamplePkg/Setup/OverClockSetup.c
/KabylakeRestrictedPkg/Library/PeiPolicyRestrictedLib/PeiCpuPolicyRestricted.c
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.c



```
/KabyLakeSiliconPkg/Cpu/Library/PeiCpuPolicyLib/PeiCpuPolicyLib.c
/KabyLakeSiliconPkg/Cpu/Library/PeiDxeSmmCpuPlatformLib/CpuPlatformLibrary.c
/KabyLakeSiliconPkg/Cpu/Library/Private/PeiCpuInitLib/CpuInitPreResetCpl.c
/KabyLakeSiliconPkg/Cpu/Library/Private/PeiCpuInitLib/Features.c
/KabyLakeSiliconPkg/Cpu/Library/Private/PeiCpuPowerMgmtLib/PowerLimits.c
/KabyLakeSiliconPkg/Cpu/Library/Private/PeiCpuPowerOnConfigLib/PeiCpuPowerOnConfigLib.c
/KabyLakeSiliconPkg/Cpu/Library/Private/PeiCpuPowerOnConfigLibDisable/PeiCpuPowerOnConfigLibDisable.c
/KabyLakeSiliconPkg/Hsti/Dxe/SecureCpuConfiguration.c
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchPm.c
/KabyLakeSvRestrictedPkg/Library/PlatformConfigXmExtLib/PackageCoreThreadElementExt.c
/KabyLakeSvRestrictedPkg/Library/PlatformConfigXmExtLib/PlatformMsrTableControlFunctions.c
```

4.1.4 Feature 4

- **Description:**
Rename FSP Structure varname to match version 2.0 draft 5
- **Solution:**
Renamed the variable names to match the name as per version 2.0 draft 5
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeFspBinPkg/DoxygenInternalOnly/DoxygenFspIntegrationGuide.h
/KabyLakeFspPkg/FspInit/Pei/FspInit.c
/KabyLakeFspPkg/FspInit/Pei/FspInit.h
/KabyLakeFspPkg/FspInit/Pei/FspInitPreMem.c
/KabyLakeFspPkg/FspInit/Pei/FspInitPreMem.h
/KabyLakeFspPkg/KabyLakeFspPkg.dec
/KabyLakeFspPkg/KabyLakeFspPkg.dsc
/KabyLakeFspPkg/KabyLakeFspPkg.fdf
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiAmtPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiCpuPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiMePolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiSaPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiSecurityPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdateLib/PeiSiPolicyUpdate.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiCpuPolicyUpdatePreMem.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiMePolicyUpdatePreMem.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiPchPolicyUpdatePreMem.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiSaPolicyUpdatePreMem.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiSecurityPolicyUpdatePreMem.c
/KabyLakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiSiPolicyUpdatePreMem.c



/KabyLakeFspPkg/Library/SerialPortLib/SerialPortLib.c
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/FspSecCore.inf
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspApiEntry.asm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspApiEntry.nasm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspApiEntry.s
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspHelper.asm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspHelper.nasm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/FspHelper.s
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/InitializeFpu.asm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/InitializeFpu.nasm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/InitializeFpu.s
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/MicrocodeLoad.inc
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/MicrocodeLoadNasm.inc
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/ResetVec.asm16#1 add
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/SaveRestoreSse.inc
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/SaveRestoreSseNasm.inc
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/Stack.asm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/Stack.nasm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/la32/Stacks.s
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/SecFsp.c
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/SecFsp.h
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/SecMain.c
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/SecMain.h
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/Vtf0/Bin/ResetVec.ia32.raw
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/Vtf0/Build.py
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/Vtf0/la16/ResetVec.asm16
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/Vtf0/ResetVectorCode.asm
/KabyLakeFspPkg/Override/IntelFspPkg/FspSecCore/Vtf0/Tools/FixupForRawSection.py
/KabyLakeFspPkg/Override/IntelFspPkg/Include/FspApi.h
/KabyLakeFspPkg/Override/IntelFspPkg/Include/Library/FspCommonLib.h
/KabyLakeFspPkg/Override/IntelFspPkg/Include/Private/FspGlobalData.h
/KabyLakeFspPkg/Override/IntelFspPkg/Library/BaseFspCommonLib/BaseFspCommonLib.inf
/KabyLakeFspPkg/Override/IntelFspPkg/Library/BaseFspCommonLib/FspCommonLib.c
/KabyLakeFspPkg/Override/IntelFspPkg/Library/BaseFspPlatformLib/BaseFspPlatformLib.inf
/KabyLakeFspPkg/Override/IntelFspPkg/Library/BaseFspPlatformLib/FspPlatformMemory.c
/KabyLakePlatSamplePkg/FspWrapperInit/FspWrapperInitApiV2.c
/KabyLakePlatSamplePkg/FspWrapperInitPreMem/FspWrapperInitPreMem.inf
/KabyLakePlatSamplePkg/FspWrapperInitPreMem/FspWrapperInitPreMemApiV2.c
/KabyLakePlatSamplePkg/Include/Library/FspPolicyInitLib.h
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspAmtPolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspCpuPolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspMePolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspPchPolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspPolicyInitLib.h
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspPolicyInitLib.inf
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspPolicyInitLibPreMem.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspSaPolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspSecurityPolicyInitLib.c
/KabyLakePlatSamplePkg/Library/PeiFspPolicyInitLib/PeiFspSiPolicyInitLib.c
/KabyLakePlatSamplePkg/PlatformPkg.dec
/KabyLakePlatSamplePkg/PlatformPkg.dsc



/KabyLakeSiliconPkg/Pch/Library/SecPchLib/SecPchLib.c
/KabyLakeSiliconPkg/Pch/Library/SecPchLib/SecPchLibFsp.inf
/KabyLakeSiliconPkg/SampleCode/Library/SecPlatformLib/SecPlatformLib.c
/KabyLakeSiliconPkg/SampleCode/Library/SecPlatformLib/SecPlatformLibFsp.inf
/KabyLakeSiliconPkg/SampleCode/SecCore/SecCoreFsp.inf

4.2 Fixed Bugs

4.2.1 Bug 1

- **Description:**
BSOD 9F Observed with ACPI.sys during S3 cycling
- **Solution:**
Fixed GPIO ASL lib incorrect macro definition caused CGLS() method not clear GPE_STS correctly
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioLib.asl

4.2.2 Bug 2

- **Description:**
FSP BIOS: Package C3 and above states are not reaching with FSP image
- **Solution:**
Resolve the SATA Port mapping code that incorrectly set the enabled just based on the setup for only FSP build
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchSata.c

4.2.3 Bug 3

- **Description:**
DCI Enable not working
- **Solution:**
Updated associated policies
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakePlatSamplePkg/Library/PeiPolicyDebugLib/PeiPchPolicyDebugPreMemLib.c
/KabyLakePlatSamplePkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdatePreMem.c



/KabyLakePlatSamplePkg/Setup/PchSetup.hfr
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/DciConfig.h

4.2.4 Bug 4

- **Description:**
Need to set NPK CTC_RESYNC bit
- **Solution:**
Set NPK CTC_RESYNC bit
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchTraceHub.c

4.2.5 Bug 5

- **Description:**
Update PCH policy description
- **Solution:**
Updated PCH policy description
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/IoApicConfig.h

4.2.6 Bug 6

- **Description:**
ChkAscii error
- **Solution:**
Fix ChkAscii error
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchScs.c

4.2.7 Bug 7

- **Description:**
SD Card SDR104 auto-tune failure
- **Solution:**
before putting 1E/5 (SDIO) to function disable, 0x834[17:16] of 1E/5 should be set to 0x10
- **Platform Affected:**
All KBL



- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchScs.c

4.2.8 Bug 8

- **Description:**
Need a BIOS DCN to Program Bit 22 of 0xfe00031C
- **Solution:**
Fixed Bit 22 programming
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchPm.c

4.2.9 Bug 9

- **Description:**
Handle both enable/disable case of CSM properly in KabylakeSiliconPkg
- **Solution:**
Use new policies to isolate and stabilize CSM enable/disable
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakePlatSamplePkg/PlatformPkg.dsc
/KabylakePlatSamplePkg/PlatformPkg.fdf
/KabylakePlatSamplePkg/PlatformPkgBuildOption.dsc
/KabylakePlatSamplePkg/PlatformPkgConfig.dsc
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.h
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.inf
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpCommon.c
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpService.c
/KabylakeSiliconPkg/Include/SiPolicyStruct.h
/KabylakeSiliconPkg/KabylakeSiliconPkg.dsc
/KabylakeSiliconPkg/Library/PeiSiPolicyLib/PeiSiPolicyLib.c
/KabylakeSiliconPkg/Library/PeiSiPolicyLib/PeiSiPolicyLib.inf
/KabylakeSiliconPkg/Library/PeiSiPolicyLib/SiPrintPolicy.c
/KabylakeSiliconPkg/Library/Private/DxeSiFvInitLib/DxeSiFvInitLib.inf
/KabylakeSiliconPkg/Library/Private/DxeSiFvInitLib/SaFvi.c
/KabylakeSiliconPkg/Me/BiosExtensionLoader/Dxe/BiosExtensionLoader.inf
/KabylakeSiliconPkg/Pch/SmartTimer/Dxe/SmartTimer.c
/KabylakeSiliconPkg/SiPkg.dec
/KabylakeSiliconPkg/SiPkgDxe.dsc
/KabylakeSiliconPkg/SiPkgDxeLib.dsc
/KabylakeSiliconPkg/SystemAgent/Include/Private/Library/LegacyRegion.h
/KabylakeSiliconPkg/SystemAgent/Library/Private/DxeLegacyRegionLib/DxeLegacyRegion.c
/KabylakeSiliconPkg/SystemAgent/Library/Private/DxeLegacyRegionLib/DxeLegacyRegionLib.inf
/KabylakeSiliconPkg/SystemAgent/Library/Private/DxeLegacyRegionLibNull/DxeLegacyRegionLibNull.c
/KabylakeSiliconPkg/SystemAgent/Library/Private/DxeLegacyRegionLibNull/DxeLegacyRegionLibNull.inf



/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/GraphicsInit.c
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/IgdOpRegion.c
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/LegacyRegion.c
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/LegacyRegion.h
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/SaInit.inf
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/SaInitUefi.c
/KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/SaInitUefi.h
/KabylakeSiliconPkg/UnitTestsInternalOnly/KabylakeUnitTestPkg.dsc



5 Version 3.7.7 Details

5.1 New Features

- None

5.2 Fixed Bugs

- None



6 Version 3.7.6 Details

6.1 New Features

- **Description:**
Set FRO bits for all PSF port configure registers
- **Solution:**
Set FRO bits for all PSF port configure registers
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPsf.h
KabylakeSiliconPkg/Pch/Library/Private/PeiDxeSmmPchPsfPrivateLib/PchPsfPrivateLib
.c

6.2 Fixed Bugs

- None



7 Version 3.7.5 Details

7.1 New Features

- **Description:**
Adding Teton Glacier (Optane) support
- **Solution:**
Added support for Hybridstorage drives
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/ConfigBlock/HybridStorageConfig.h
KabylakeSiliconPkg/Pch/Include/PchPolicyCommon.h
KabylakeSiliconPkg/Pch/Include/Private/Library/PeiHybridStorageLib.h
KabylakeSiliconPkg/Pch/Include/Private/Ppi/HybridStoragePpi.h
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.inf
KabylakeSiliconPkg/Pch/Library/Private/PeiHybridStorageLib/PeiHybridStorageLib.c
KabylakeSiliconPkg/Pch/Library/Private/PeiHybridStorageLib/PeiHybridStorageLib.inf
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInit.c
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PeiPchInitLib.inf
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PeiPchInitLibFsp.inf

7.2 Fixed Bugs

- None



8 Version 3.7.4 Details

8.1 New Features

- None

8.2 Fixed Bugs

- None



9 Version 3.7.3 Details

9.1 New Features

- None

9.2 Fixed Bugs

9.2.1 Bug 1

- **Description:**
Revert set EgressFRO/IngressFRO for all PSF
- **Solution:**
Revert set FRO bits for PSF Port Config registers which was introduced in v3.7.1.
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPsf.h
KabylakeSiliconPkg/Pch/Library/Private/PeiDxeSmmPchPsfPrivateLib/PchPsfPrivateLib.c



10 Version 3.7.2 Details

10.1 New Features

- None

10.2 Fixed Bugs

- None

10.2.1 Bug 1

- **Description:**
xHCI programming doesn't enable USB3 Port Clock Gating feature
- **Solution:**
Enable USB3 Port Clock Gating feature by clearing BIT16 in AUX_CTRL_REG1
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchUsb.c

10.2.2 Bug 2

- **Description:**
PchHdaAcpi causes access to NULL pointer
- **Solution:**
Fix definition
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchHdaAcpi.c



11 Version 3.7.1 Details

11.1 New Features

- None

11.2 Fixed Bugs

11.2.1 Bug 1

- **Description:**
Need to Set EgressFRO/IngressFRO for all PSF
- **Solution:**
Set FRO bits for PSF Port Config registers.
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPsf.h
KabylakeSiliconPkg/Pch/Library/Private/PeiDxeSmmPchPsfPrivateLib/PchPsfPrivateLib.c



12 Version 3.7.0 Details

12.1 New Features

12.1.1 Feature 1

- **Description:**
Update eMMC “Rx_CMD_Data_dly_2” default setting, and restore “cmd_data_sdr104_hs200” DLL register with auto tuning value multiply by 2 on eMMC D3 entry.
- **Solution:**
N/A
- **Platform Affected:**
SKL-LP/KBL-LP
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl
KabylakeSiliconPkg/Pch/Include/PchReservedResources.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsScs.h
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchScs.

12.2 Fixed Bugs

12.2.1 Bug 1

- **Description:**
S4 cycle hang with post code = 00AD/00B4/0096 while enable “Time and Alarm Device” ACPI device.
- **Solution:**
Disable WADT_EN bit while booting.
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmmCore.c
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchxSmmHelpers.c
KabylakeSiliconPkg/Pch/SmmControl/RuntimeDxe/SmmControlDriver.c

12.2.2 Bug 2

- **Description:**
I2C device which is connected to I2C 2/3/4/5 controllers may lose function after wake up from modern standby.



- **Solution:**
I2C 2/3/4/5 does not support 3.3V (only 1.8V), due to GPIO GPP_F limitation.
BIOS has to clear PAD_CFG_DW1_GPP_F_4~11[25] for I2C 2/3/4/5.
- **Platform Affected:**
SKL-LP/KBL-LP
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/ConfigBlock/SerialIoConfig.h
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchSerialIoLib/PeiDxeSmmPchSerialIoLib.
c

12.2.3 Bug 3

- **Description:**
USB wake not happening from TBT2/TBT3 docks.
- **Solution:**
Enabling Tire2 GPIO Wake Capability while entering into Sx.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl



13 Version 3.6.9 Details

13.1 New Features

- None

13.2 Fixed Bugs

- None



14 Version 3.6.8 Details

14.1 New Features

- None

14.2 Fixed Bugs

- None



15 Version 3.6.7.1 Details

15.1 New Features

- None

15.2 Fixed Bugs

- None



16 Version 3.6.7 Details

16.1 New Features

16.1.1 Feature 1

- **Description:**
Add D3 PEP constraint for PCH CSI2 camera device.
- **Solution:**
N/A
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl

16.1.2 Feature 2

- **Description:**
Port ACPI Time and Alarm Device (TAD) support.
- **Solution:**
N/A
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl

16.2 Fixed Bugs

16.2.1 Bug 1

- **Description:**
System hang while connecting NvmExpressDxe driver if 8259 driver is not included
- **Solution:**
Disable 8259 hardware interrupts in SiliconPkg
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInitPreMem.c



16.2.2 Bug 2

- **Description:**
Update link active check timeout
- **Solution:**
Slp_S0 is not working with Intel Wireless-AC 9260(Thunder Peak)
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

16.2.3 Bug 3

- **Description:**
AbCS/00CS Hung observed during CS cycling
- **Solution:**
Clear IO Trap Status every time the enable bit is cleared
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/loTrap.c

16.2.4 Bug 4

- **Description:**
- **Solution:**
- **Platform Affected:**
All KBL
- **Affected Files:**



17 Version 3.6.6 Details

17.1 New Features

- None

17.2 Fixed Bugs

- None



18 Version 3.6.6 Details

18.1 New Features

18.1.1 Feature 1

- **Description:**
B365 PCH SKU addition for CFL-S
- **Solution:**
N/A
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

18.1.2 Feature 2

- **Description:**
SKU addition for AML-Y 2+2
- **Solution:**
N/A
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Cpu/Library/Private/PeiCpuInitLib/CpuInitPreResetCpl.c

18.2 Fixed Bugs

18.2.1 Bug 1

- **Description:**
Include Tjmax offset programming in the S3 reset handling
- **Solution:**
Update PmcLib services to PmcSetBclkS3(), PmcClearBclkS3(), PmcIsBclkS3Boot()
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Cpu/Library/Private/PeiCpuOclnitLib/CpuOclnit.c
KabylakeSiliconPkg/Cpu/Library/Private/PeiCpuOclnitLib/PeiCpuOclnitLib.inf
KabylakeSiliconPkg/Pch/Include/Library/PchPmcLib.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPmc.h



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KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchPmcLib/PchPmcLib.c
KabylakeSiliconPkg/SystemAgent/Library/Private/PeiSaOcInitLib/PeiSaOcInitLib.c
KabylakeSiliconPkg/SystemAgent/Library/Private/PeiSaOcInitLib/PeiSaOcInitLib.inf



19 Version 3.6.5 Details

19.1 New Features

- None

19.2 Fixed Bugs

19.2.1 Bug 1

- **Description:**
Slp_S0 does not work with Intel Wireless-AC 9260 and PCIe speed set to Auto
- **Solution:**
Fixed endpoint programming to align with configuration expectations.
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c



20 Version 3.6.4 Details

20.1 New Features

20.1.1 Feature 1

- **Description:**
Disable clock when disabling the PCIe Root Port
- **Solution:**
Created UPD to allow users to forcefully disable clock
- **Platform Affected:**
All KBL
- **Affected Files:**
 - KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
 - KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
 - KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

20.2 Fixed Bugs

- None



21 Version 3.6.3 Details

21.1 New Features

- None

21.2 Fixed Bugs

- None



22 Version 3.6.2 Details

22.1 New Features

- None

22.2 Fixed Bugs

- None



23 Version 3.6.1.1 Details

23.1 New Features

- None

23.2 Fixed Bugs

- None



24 Version 3.6.1 Details

24.1 New Features

24.1.1 Feature 1

- **Description:**
BIOS must set TCO_BASE_LOCK bit in the TCOCTL register
- **Solution:**
Set TCO_BASE_LOCK bit in the TCOCTL register
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchCycleDecodingLib/PchCycleDecodingLib.c

24.2 Fixed Bugs

- None



25 Version 3.6.0 Details

25.1 New Features

- None

25.2 Fixed Bugs

- None



26 Version 3.5.0 Details

26.1 New Features

26.1.1 Feature 1

- **Description:**
Updated channel mask value for DMIC based on HDA driver requirement
- **Solution:**
Updated channel mask in DMIC format for channel 2 and 4
- **Platform Affected:**
All KBL
- **Affected Files:**
`/KabylakeSiliconPkg/Pch/Library/Private/DxePchHdaLib/PchHdaEndpoints.c`

26.2 Fixed Bugs

- **None**



27 Version 3.4.0 Details

27.1 New Features

- None

27.2 Fixed Bugs

- None



28 Version 3.3.1 Details

28.1 New Features

- None

28.2 Fixed Bugs

- None



29 Version 3.3.0 Details

29.1 New Features

- None

29.2 Fixed Bugs

- None



30 Version 3.2.1 Details

30.1 New Features

- None

30.2 Fixed Bugs

- None



31 Version 3.2.0 Details

31.1 New Features

31.1.1 Feature 1

- **Description:**
Added support for H310C PCH SKU
- **Solution:**
Updated H310C string name
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

31.2 Fixed Bugs

31.2.1 Bug 1

- **Description:**
Knob "Disable PCH WATCHDOG Timer" stopped working
- **Solution:**
Updated Wdt disable logic to lock the register when wdt is disabled.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/Wdt.c

31.2.2 Bug 2

- **Description:**
Default LTR Max Snoop/ Non-Snoop Latency settings need alignment
- **Solution:**
Default LtrMax policy for PCH-H chipsets was assigned in an inconsistent way
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakePlatSamplePkg/Library/PeiPolicyDebugLib/PeiPchPolicyDebugLib.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c



31.2.3 Bug 3

- **Description:**
LTE: Hang on Desktop/Black Screen Exiting CS During PST (USB)
- **Solution:**
Update XHCI asl
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl

31.2.4 Bug 4

- **Description:**
BIOS doesn't wait for xDCI to power gate fully
- **Solution:**
Updated power gating code
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchXdci.c



32 Version 3.1.2 Details

32.1 New Features

32.1.1 Feature 1

- **Description:**
Provide BCFS (BIOS control feature support) to disable and enable CPU Attached Storage for Z370
- **Solution:**
Added a policy to program BIT14 in RST feature mask register.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SataConfig.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsSata.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchSata.c

32.2 Fixed Bugs

- **None**



33 Version 3.1.1 Details

33.1 New Features

- None

33.2 Fixed Bugs

33.2.1 Bug 1

- **Description:**
High CPU & PCH power in IDLE Display
- **Solution:**
Updated PEG ASL
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/SystemAgent/AcpiTables/PegSsdt/PegOnOff.asl

33.2.2 Bug 2

- **Description:**
Cannot recognize Mobile phone via USB 3.0 and USB Type-C port
- **Solution:**
Set MSE bit instead of BME bit for PMC.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchPm.c



34 Version 3.0.1 Details

34.1 New Features

- None

34.2 Fixed Bugs

- None



35 Version 3.0.0 Details

35.1 Fixed Bugs

35.1.1 Bug 1

- **Description:**
PCIe hotplug event (_L61) keeps being triggered by Thunderbolt after system resuming from S3/S4 state
- **Solution:**
Add PCIe root port hotplug SCI event enable/disable policy
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

35.1.2 Bug 2

- **Description:**
Fix some PCIe device might not be enumerated when hotplugging/unplugging PCIe device at S3/S4 state
- **Solution:**
Change back PCIE root port configuration space type to PCI configuration instead of system memory configuration
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchPcie.asl

35.1.3 Bug 3

- **None**



36 Version 2.9.2 Details

36.1 Fixed Bugs

36.1.1 Bug 1

- **Description:**
For platform design without SLP_S0# voltage margining and enable WOV feature, SLP_S0# cannot be asserted
- **Solution:**
BIOS set PWRMBASE + 0x31C [22] to 1b
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchPm.c

36.1.2 Bug 2

- **Description:**
Serial debug message via PCH UART might lost due to it won't return bytes unless the buffer is full
- **Solution:**
Check break interrupt bit of Line status register. If not set, copy the byte into receive buffer.
- **Platform Affected:**
All KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchSerialIoUartLib/PeiDxeSmmPchSerialIoUartLib.c



37 Version 2.9.0 Details

37.1 Fixed Bugs

37.1.1 Bug 1

- **Description:**
Request conditional delay for PCIE devices
- **Solution:**
Added delay in PCIE device detection
- **Platform Affected:**
All KBL
- **Affected Files:**
`/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c`

37.1.2 Bug 2

- **None**

38 Version 2.8.1 Details

38.1 Fixed Bugs

38.1.1 Bug 1

- **Description:**
Issue with Pleasentstar NVMe SSD enumeration
- **Solution:**
Improved rootport device connected logic
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

38.1.2 Bug 2

- **Description:**
Yellow Bang on Internal GbE
- **Solution:**
Updated clkreq assignment policy
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakePlatSamplePkg/Board/Others/PeiBoardInitLib/OthersBoardPchInitPreMemLib.c
/KabylakePlatSamplePkg/Board/SkylakeA0Rvp3/PeiBoardInitLib/PeiSkylakeA0Rvp3InitPreMemLib.c
/KabylakePlatSamplePkg/Board/SkylakeURvp7/PeiBoardInitLib/PeiSkylakeURvp7InitPreMemLib.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h

38.1.3 Bug 3

- **Description:**
PCIe clocks disabled along with disabled rootports blocking SLP_S0#
- **Solution:**
Changed programming on PCIe CLKREQ Control for Disabled Port
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c



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/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

38.1.4 Bug 4

- **Description:**
No CSME PG until first TPM driver command
- **Solution:**
Added code to put PTT in idle after this command.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Me/Library/Private/PeiMeInitLib/PchMeUma.c



39 Version 2.8.0 Details

39.1 New Features

None

39.2 Fixed Bugs

39.2.1 Bug 1

- **Description:**
LTR and OBFF settings not properly mapped to PCIe_DSM
- **Solution:**
Add new local variables to properly distribute settings
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchPcie.asl



40 Version 2.7.2 Details

40.1 New Features

40.1.1 Feature 1

- **Description:**
Setup xHCI DbC for Trace Hub tracing
- **Solution:**
Program xhci dbc_trace registers on boot by FW agent
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsPcr.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsTraceHub.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchSbiAccessLib/PchSbiAccessLib.c
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmTraceHubInitLib/PeiDxeSmmTraceHubInitLib.c
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmTraceHubInitLib/PeiDxeSmmTraceHubInitLib.inf

40.1.2 Feature 2

- **Description:**
Provide UPD to control the flash configuration lock down.
- **Solution:**
Change SPI FLASH_CONFIGURATION_LOCKDOWN (FLOCKDN) register
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakePlatSamplePkg/FspWrapper/Library/PeiFspPolicyInitLib/PeiFspPchPolicyInitLib.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PchRestrictedConfig.h
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SpiConfig.h
/KabylakeSiliconPkg/Pch/Include/Private/PchConfigHob.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInit.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c



40.2 Fixed Bugs

- None



41 Version 2.7.0 Details

41.1 New Features

41.1.1 Feature 1

- **Description:**
Enable SLP_S0 with LPA and display ON on KBL R
- **Solution:**
New Voltage Margining flow supporting also discrete VR controlled by GPIO
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl

41.1.2 Feature 2

- **Description:**
Hide PCH-IO Configuration / PMC Read
- **Solution:**
Disable BIOS SETUP option
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c

41.1.3 Feature 3

- **Description:**
Enable Energy reporting feature by default
- **Solution:**
Enable Energy reporting feature by default
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h



/KabyLakeSiliconPkg/Pch/Include/Private/PchConfigHob.h
/KabyLakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c

41.1.4 Feature 4

- **Description:**
Align WRSDIS implementation across segments.
- **Solution:**
Set Bit 11 in SPIBAR+0x04
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c

41.2 Fixed Bugs

41.2.1 Bug 1

- **Description:**
Align WWAN PEWAKE on KBL-Y RVP3
- **Solution:**
Change initial setting of WWAN PEWAKE
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLib.c

41.2.2 Bug 2

- **Description:**
The HSTI test failed when PMC_READ_DISABLED is set to Disabled.
- **Solution:**
Let OEM to enable or disable appropriately.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Hsti/Dxe/SecurePCHConfiguration.c

41.2.3 Bug 3

- **Description:**
TBAR + 40h not programmed when manual setting TT.
- **Solution:**
Fixed programming for TBAR + 40h



Version 3.8.0 Details

- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchThermal.c



42 Version 2.6.2 Details

42.1 New Features

None

42.2 Fixed Bugs

42.2.1 Bug 1

- **Description:**
SUT hangs at Intel logo screen with PCA7 after enabling Overclocking
- **Solution:**
Updated WDT disable conditions
- **Platform Affected:**
All KBL
- **Affected Files:**
`/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchWdtCommonLib/WdtCommon.c`



43 Version 2.6.1 Details

43.1 New Features

None

43.2 Fixed Bugs

43.2.1 Bug 1

- **Description:**
No Runtime D3 (RTD3) support for PCH SDCard
- **Solution:**
Added _S0W to PSDC for RTD3.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl



44 Version 2.6.0 Details

44.1 New Features

None

44.2 Fixed Bugs

44.2.1 Bug 1

- **Description:**
USB docking/device plug in/out cause system hang during burn-in test.
- **Solution:**
BIOS should refer to CAS bit before set/clear D3HE bit while XHCI D0/D3 entry and in Sx handler.
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.c
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchXhciSxSmm.c

44.2.2 Bug 2

- **Description:**
Correct KBL PCH-H Server/WS naming for X299 and C422.
- **Solution:**
Updated string
- **Platform Affected:**
KBL-H
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

44.2.3 Bug 3

- **Description:**
BIOS to avoid clear FCERR bit when setting FLOCKDN and WRSDIS bits.
- **Solution:**
Write only required lock bits to the register with 2 byte write access.
- **Platform Affected:**



Version 3.8.0 Details

All KBL

- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c



45 Version 2.5.1 Details

45.1 New Features

None

45.2 Fixed Bugs

45.2.1 Bug 1

- **Description:**
Production signed BiG module should be compatible with KBL PCH
- **Solution:**
Update to Include production signed Bios Guard binary
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakePlatSamplePkg/PlatformInit/PlatformInitPei/PlatformInit.c
/KabyLakePlatSamplePkg/PlatformInit/PlatformInitPei/PlatformInit.inf
/KabyLakeSiliconPkg/Cpu/BiosGuard/Smm/BiosGuardServices.c
/KabyLakeSiliconPkg/Cpu/BiosGuard/Smm/BiosGuardServices.inf
/KabyLakeSiliconPkg/Cpu/Include/BiosGuard.h
/KabyLakeSiliconPkg/Cpu/Include/Library/CpuPlatformLib.h
/KabyLakeSiliconPkg/Cpu/Library/PeiDxeSmmCpuPlatformLib/CpuPlatformLibrary.c
/KabyLakeSiliconPkg/Pch/Include/Library/PchWdtCommonLib.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchWdtCommonLib/WdtCommon.c



46 Version 2.5.0 Details

46.1 New Features

46.1.1 Feature 1

- **Description:**
 - Set WRSDIS bit in SPI flash controller as security recommendation
- **Solution:**
 - Disable Write Status command as a security concern
- **Platform Affected:**
 - All KBL
- **Affected Files:**
 - /KabylakeSiliconPkg/Pch/Include/Register/PchRegsSpi.h
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c

46.2 Fixed Bugs

46.2.1 Bug 1

- **Description:**
 - Fail to build KBL code base with VS2012
- **Solution:**
 - Fixed uninitialized variable
- **Platform Affected:**
 - All KBL
- **Affected Files:**
 - /KabylakeSiliconPkg/Hsti/Dxe/SecurePCHConfiguration.c



47 Version 2.4.0 Details

47.1 New Features

None

47.2 Fixed Bugs

None



48 Version 2.2.1 Details

Production Version Update

48.1 New Features

None

48.2 Fixed Bugs

48.2.1 Bug 1

- **Description:**
USB2 devices may not enumerate correctly or yellow bang after resuming from S3.
- **Solution:**
Force PLL cycle bit in PLL2 register is set if detected that USB2 PLL didn't lock properly

*For detailed information, please refer to Sighting#1209950976 in **Doc#572342 – Kaby Lake Refresh Platform Sighting Report rev 2.0.***

- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchUsb.c

48.2.2 Bug 2

- **Description:**
Change PCH Thermal Device to disable or Enable in ACPI mode would hang
- **Solution:**
Improved TBAR initialization logic to be more robust
- **Platform Affected:**
All KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Hsti/Dxe/SecurePCHConfiguration.c

48.2.3 Bug 3

- **Description:**
Sometimes system will hang at BIOS POST Code "04" after resume from S3



- **Solution:**
On KBL-H platform, BIOS should not touch AUX_CTRL_REG[10] in PchXhciS3Callback() and XhciHcInit().
- **Platform Affected:**
KBL-H
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchUsb.c
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchXhciSxSmm.c



49 Version 2.3.0 Details

Production Version Update

49.1 New Features

49.1.1 Feature 1

- **Description:**
Add Z370 PCH support
- **Solution:**
Updated device list and strings
- **Platform Affected:**
KBL-H
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

49.2 Fixed Bugs

49.2.1 Bug 1

- **Description:**
Enable or disable PCH Thermal Device in ACPI mode would hang
- **Solution:**
Logic added to better manage state transitions
- **Platform Affected:**
All KBL
- **Affected Files:**
/2016_Kabylake/KabylakeSiliconPkg/Hsti/Dxe/SecurePCHConfiguration.c



50 Version 2.2.0 Details

Production Version Update

50.1 New Features

50.1.1 Feature 1

- **Description:**
Provide disable/enable System Acceleration with Optane Memory
- **Solution:**
Add policy to enable/disable Optane(TM)
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SataConfig.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsSata.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c

50.2 Fixed Bugs

50.2.1 Bug 1

- **Description:**
Glitch noise issue in the system having HD-A and USB type-C
- **Solution:**
Mitigated delay from SMI rootport training
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabylakePlatSamplePkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchPcieSmm.c



50.2.2 Bug 2

- **Description:**
GPIO_DIRECTION setting not updated when pad is configured for output or has RX&TX buffers disabled
- **Solution:**
Corrected GPIO_DIRECTION after reading PADCFG_DW0 register
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLib.c



51 Version 2.1.0 Details

Production Version Update

51.1 New Features

51.1.1 Feature 1

- **Description:**
Added Chrome support for HDMI Audio
- **Solution:**
Chrome requires Disp/HDMI codec detection to operate in I2S mode.
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchHda.c

51.2 Fixed Bugs

51.2.1 Bug 1

- **Description:**
TBARB define in HSTI caused read HSTI SPI lock status failure
- **Solution:**
Changed TBARB width to 64bit
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
KabylakeSiliconPkg/Hsti/Dxe/SecurePCHConfiguration.c

52 Version 2.0.0 Details

Production Version Update

52.1 New Features

52.1.1 Feature 1

- **Description:**
DciAutoDetect is deprecated
- **Solution:**
Remove DciAutoDetect to prevent accidental use
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInitPreMem.c
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchPm.c

52.2 Fixed Bugs

52.2.1 Bug 1

- **Description:**
USB does not wake from S3 with Debug mode enabled
- **Solution:**
Workaround with 0xA2[2], 0x50[2] in SMI Handler
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
/KabyLakeSiliconPkg/Pch/PchInit/Smm/PchXhciSxSmm.c

52.2.2 Bug 2

- **Description:**
ESPI not initialized in EFI shell
- **Solution:**
Set BME bit for both Master and slave devices under eSPI
- **Platform Affected:**
KBL U/Y



- **Affected Files:**
 - /KabylakeSiliconPkg/Pch/Include/ConfigBlock/EspiConfig.h
 - /KabylakeSiliconPkg/Pch/Include/PchPolicyCommon.h
 - /KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
 - /KabylakeSiliconPkg/Pch/Include/Register/PchRegsSpi.h
 - /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
 - /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
 - /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.inf
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.h
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.inf
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxeFsp.inf
 - /KabylakeSiliconPkg/SiPkg.dec

52.2.3 Bug 3

- **Description:**

Program PchSmmCoreRegister with exact size to avoid buffer overflow.
- **Solution:**

Updated programming in DispatchHandle
- **Platform Affected:**

KBL U/Y
- **Affected Files:**
 - /KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmmCore.c

52.2.4 Bug 4

- **Description:**

SUT hangs with Lock Enable (LE) Bit to 0 and Write Protect Disable (WPD) bit to 1
- **Solution:**

BIOS should handle WPD SMI for LPC/eSPI/SPI
- **Platform Affected:**

KBL U/Y
- **Affected Files:**
 - /KabylakeSiliconPkg/Pch/Include/Library/PchEspiLib.h
 - /KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
 - /KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchEspiLib/PchEspiLib.c
 - /KabylakeSiliconPkg/Pch/PchInit/Smm/PchBiosWriteProtect.c
 - /KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
 - /KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.inf
 - /KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmiDispatch.c
 - /KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmiDispatcher.inf
 - /KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmm.h
 - /KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmmEspi.c



53 Version 1.9.0 Details

Production Version Update

53.1 New Features

53.1.1 Feature 1

- **Description:**
Added eMMC_DSM Function 9 of SDBUS driver
- **Solution:**
Added Driver Strength value (set by PchPolicy) to OS driver.
- **Platform Affected:**
KBL U/Y
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/ScsConfig.h
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchAcpi.c

53.2 Fixed Bugs

None



54 Version 1.8.0 Details

Production Version Update

54.1 New Features

54.1.1 Feature 1

- **Description:**
Set DCI “Host EXI Enable Lock” bit, and deprecated “DciAutoDetect” BIOS policy to increase platform security.
- **Solution:**
Set Host EXI Enable Lock (HOST_EXI_EN_LOCK) as default, and remove “DciAutoDetect” BIOS policy.
- **Platform Affected:**
All KBL SKUs
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/DciConfig.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsDci.h

54.2 Fixed Bugs

54.2.1 Bug 1

- **Description:**
AMT_024 Remote Graceful shutdown doesn't work
- **Solution:**
Remove internal only tags and use CondRefOf for HIDWAKEDSM.asl
- **Platform Affected:**
All KBL SKUs
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHeci.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchIsh.asl

54.2.2 Bug 2

- **Description:**
PciePIIScc is not properly initialized
- **Solution:**
Fixed Policy variable initialization



Version 3.8.0 Details

- **Platform Affected:**
All KBL SKUs
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPreMemPolicyLib.c



55 Version 1.7.0 Details

Production Version Update

55.1 New Features

55.1.1 Feature 1

- **Description:**
Add native MSFT OS support / OS Downgrade/upgrade support
- **Solution:**
Add Setup switch to Enable/Disable TBT Real native.
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchPcie.asl

55.2 Fixed Bugs

None



56 Version 1.6.0 Details

Production Version Update

56.1 New Features

56.1.1 Feature 1

- **Description:**
Add support for QMS185 and C422A SKUs
- **Solution:**
Updated info - 0xa156 is another flavor of SPT SFF
- **Platform Affected:**
KBL-H/S
- **Affected Files:**

/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

56.1.2 Feature 2

- **Description:**
Create separate FV Segment for FSP-S
- **Solution:**
Create FSP-S as a separated FV segment, and do signature verification, before proceeding for SecureBootEnable
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabyLakeFspPkg/KabyLakeFspPkg.fdf

56.1.3 Feature 3

- **Description:**
Add SVENTX Catalog messages for release BIOS
- **Solution:**
Added NPK output hook to ADBG method.
- **Platform Affected:**
KBL-H/S



- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/TraceHubDebug.asl

56.2 Fixed Bugs

56.2.1 Bug 1

- **Description:**
SpiEiss and BiosLock are not set with BIOS Guard during capsule update flow.
- **Solution:**
Fixed SpiEiss and BiosLock logic
- **Platform Affected:**
All
- **Affected Files:**
/KabylakePlatSamplePkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c

56.2.2 Bug 2

- **Description:**
FSP VS BIOS hangs at PC 9b47
- **Solution:**
Reduced 4K from FspTemporaryRamSize to accommodate the req.
- **Platform Affected:**
All
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc

56.2.3 Bug 3

- **Description:**
With FSP, Processor trace memory values are not maintained after S3 resume
- **Solution:**
Use HOB and PCDs to save and restore Processor Trace S3 resume data in FSP
- **Platform Affected:**
All
- **Affected Files:**
KabylakeFspPkg/KabylakeFspPkg.dsc
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.inf
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpService.c
KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
KabylakeSiliconPkg/SiPkg.dec



56.2.4 Bug 4

- **Description:**
W/A for DPIB status write
- **Solution:**
Always update DPIB status at the end of the HD-A 48 KHz frame
- **Platform Affected:**
All
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchHda.c

56.2.5 Bug 5

- **Description:**
Audio recording functionality is not working after S3
- **Solution:**
Added macro to populate structure size automatically.
- **Platform Affected:**
All
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h



57 Version 1.5.0 Details

Production Version Update

57.1 New Features

- **None**

57.2 Fixed Bugs

57.2.1 Bug 1

- **Description:**
Revert back eMMC_DSM Function 9 introduced in Rev 1.3.0
- **Solution:**
n/a
- **Platform Affected:**
All
- **Affected Files:**
/ClientBIOS/2016_Kabylake/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl
/ClientBIOS/2016_Kabylake/KabylakeSiliconPkg/Pch/Include/ConfigBlock/ScsConfig.h
/ClientBIOS/2016_Kabylake/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchAcpi.c



58 Version 1.4.2 Details

Production Version Update

58.1 New Features

- **None**

58.2 Fixed Bugs

58.2.1 Bug 1

- **Description:**
Root Port Destination ID data misses values for KBL-PCH-H
- **Solution:**
Updated PCH RC Cycle decoding lib with KBL-PCH-H specific values
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchCycleDecodingLib/PchCycleDecodingLib.c

58.2.2 Bug 2

- **Description:**
FSP, Processor trace memory values are not maintained after S3 resume
- **Solution:**
Added HOB and PCDs to save and restore Processor Trace S3 resume data in FSP
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakePlatSamplePkg/FspWrapper/Library/PeiFspPolicyInitLib/PeiFspCpuPolicyInitLib.c
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.inf
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpService.c
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
/KabylakeSiliconPkg/SiPkg.dec



59 Version 1.4.1 Details

Production Version Update

59.1 New Features

59.1.1 Feature 1

- **Description:**
Add BSOD dump data for RAID/SRT device
- **Solution:**
Add BCCD entry and _DEP method for RST RAID volumes
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSata.asl

59.1.2 Feature 2

- **Description:**
Add a policy for disabling USB disabled in PEI phase
- **Solution:**
Created new policy
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/UsbConfig.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitFsp.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.c

59.2 Fixed Bugs

59.2.1 Bug 1

- **Description:**



System hang at windows logo during install Win7 x64 OS on NVME

- **Solution:**
Changed SATA.EGCR.TSCAS programming
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

59.2.2 Bug 2

- **Description:**
ResetShutdown() routine, power button status clear is not done properly
- **Solution:**
Clear PM1_EN_STS register BIT8
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/BaseResetSystemLib/BaseResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/DxeResetSystemLib/DxeResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c

59.2.3 Bug 3

- **Description:**
NVME device lost when system resume from S3 state
- **Solution:**
Added SATA.EGCR programming for Optane memory to S3 boot script
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c



60 Version 1.4.0 Details

Production Version Update

60.1 New Features

60.1.1 Feature 1

- **Description:**
Add setup option to disable WDT
- **Solution:**
Watchdog timer using new setup option added
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchWdtCommonLib/PeiDxeSmmPchWdtCommonLib.inf
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchWdtCommonLib/WdtCommon.c
/KabylakeSiliconPkg/SiPkg.dec

60.1.2 Feature 2

- **Description:**
Architect PchVerbTable structure to allow auto compute of array size
- **Solution:**
Refactored HDA verb table handling to use sizeof operator
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h

60.1.3 Feature 3

- **Description:**
Augment legacy IO low latency mode for some robotic applications
- **Solution:**
Added a platform policy and setup option for "Legacy IO Low Latency mode"
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c



/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/DmiConfig.h
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsP2sb.h
/KabyLakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

60.1.4 Feature 4

- **Description:**
Disable resets while booting
- **Solution:**
Add setup option to disable resets while booting
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabyLakeFspPkg/KabyLakeFspPkg.dsc
/KabyLakeSiliconPkg/Me/BiosExtensionLoader/Dxe/BiosExtensionLoader.c
/KabyLakeSiliconPkg/Me/BiosExtensionLoader/Dxe/BiosExtensionLoader.inf
/KabyLakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.c
/KabyLakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.inf
/KabyLakeSiliconPkg/Pch/Library/PeiPchResetLib/PchReset.c
/KabyLakeSiliconPkg/Pch/Library/PeiPchResetLib/PeiPchResetLib.inf
/KabyLakeSiliconPkg/SiPkg.dec

60.1.5 Feature 5

- **Description:**
Use LPC as default HPET and IOxAPIC requester/completer ID
- **Solution:**
Remove the programming HBDF in P2SB.
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabyLakeFspPkg/KabyLakeFspPkg.dsc
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/HpetConfig.h
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/IOApicConfig.h
/KabyLakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchSamplePolicyLib.c
/KabyLakeSiliconPkg/SystemAgent/AcpiTables/Dmar/Dmar.aslc
/KabyLakeSiliconPkg/SystemAgent/SalNit/Dxe/VTd.c

60.1.6 Feature 6

- **Description:**
Add new programming for XHCLKGTEN
- **Solution:**
Added new programming and exposed the functionality in ASL
- **Platform Affected:**
KBL-H/S



- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl

60.1.7 Feature 7

- **Description:**
Provide eMMC _DSM Function 9 as part of SDBUS driver
- **Solution:**
Added eMMC _DSM Function 9 to Driver Strength value
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/ScsConfig.h
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchAcpi.c
/KabylakeSiliconPkg/SiNvsInternalOnly/PchNvs.aht

60.1.8 Feature 8

- **Description:**
Update USB3 PDO flow for BIOS
- **Solution:**
New PDO setting flow was implemented
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h

60.1.9 Feature 9

- **Description:**
Disable PSF address-based peer-to-peer decoding by default
- **Solution:**
Clear PSF_<x>_ROOTSPACE_CONFIG_RS<0/1> by default
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsPsf.h

60.1.10 Feature 10

- **Description:**
Support SSC programming and PciePIISsc config block entry to pre-mem
- **Solution:**
Moved SSC programming and PciePIISsc config block entry to pre-mem
- **Platform Affected:**



KBL-H/S

- **Affected Files:**

- /KabylakeFspPkg/KabylakeFspPkg.dsc
- /KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
- /KabylakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiPchPolicyUpdatePreMem.c
- /KabylakeSiliconPkg/Pch/Include/ConfigBlock/HsioPcieConfig.h
- /KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
- /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPreMemPrintPolicy.c
- /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
- /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchSamplePreMemPolicyLib.c
- /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c

60.2 Fixed Bugs

60.2.1 Bug 1

- **Description:**

Wrong GPIO ACPI Device ID on KBL PCH-H

- **Solution:**

Updated GPIO ACPI Device ID

- **Platform Affected:**

KBL-H/S

- **Affected Files:**

- /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSeriallo.asl
- /KabylakeSiliconPkg/Pch/Include/Register/PchRegsSeriallo.h

60.2.2 Bug 2

- **Description:**

GPIO 2-tier GPE handling (_L6F) may miss an event

- **Solution:**

Each 2-Tier will have its status cleared separately by the handler of this event.

- **Platform Affected:**

KBL-H/S

- **Affected Files:**

- /KabylakePlatSamplePkg/Acpi/AcpiTables/Dsdt/Gpe.asl
- /KabylakePlatSamplePkg/Acpi/AcpiTables/SsdtRtd3/Rvp3Rtd3.asl
- /KabylakePlatSamplePkg/Acpi/AcpiTables/SsdtRtd3/Rvp3Sku31Rtd3.asl
- /KabylakePlatSamplePkg/Acpi/AcpiTables/SsdtRtd3/Rvp7Rtd3.asl
- /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioLib.asl
- /KabylakeSiliconPkg/SystemAgent/AcpiTables/PegSsdt/PegOnOff.asl
- /KabylakeSiliconPkg/SystemAgent/AcpiTables/PegSsdt/PegSsdt.asl



60.2.3 Bug 3

- **Description:**
GNL-R RSTe OpROM is not dispatch
- **Solution:**
Added RaidDeviceId option
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SataConfig.h
/KabylakeSiliconPkg/Pch/Include/Library/PchInfoLib.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c

60.2.4 Bug 4

- **Description:**
BCLK values are not reflecting correctly
- **Solution:**
Moved WDT reset check
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Library/OcWdtLib.h
/KabylakeSiliconPkg/Pch/Library/PeiOcWdtLib/PeiOcWdtLib.c

60.2.5 Bug 5

- **Description:**
Cm/Cp values are lost after S3 exit
- **Solution:**
Updated value written to EQCFG register on S3 resume
- **Platform Affected:**
KBL-H/S
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.c



61 Version 1.3.0 Details

No change in this version.



62 Version 1.2.0 Details

Production Version Update

62.1 New Features

62.1.1 Feature 1

- **Description:**

Update KBL PCH Chipsetinit table to Rev.11.

For more details, please refer to “Doc#569614 – Intel 200 Series Chipset (Kaby Lake-S PCH-H) – Electrical Settings Sighting#4774031”.

- **Solution:**

Update Chipsetinit table.

Platform Affected:

KBL-H/S

- **Affected Files:**

KabylakeSiliconPkg\Pch\Library\Private\PeiPchInitLib\KblPchHHsioAx.c

KabylakeSiliconPkg\Pch\Include\Private\KblPchHHsioAx.h

62.2 Fixed Bugs

None



63 Version 1.1.0 Details

Production Version Update

63.1 New Features

63.1.1 Feature 1

- **Description:**
Added support for BSOD data dump for RST device
- **Solution:**
Add BCCD entry and _DEP method for RST RAID volumes
Platform Affected:
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSata.asl

63.2 Fixed Bugs

63.2.1 Bug 1

- **Description:**
SATAGC.AIE not set when Alternate ID is enabled for SATA Controller
- **Solution:**
Added policy check and set AIE bit accordingly
Platform Affected:
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsSata.h

63.2.2 Bug 2

- **Description:**
RTD3 support for SATA devices is incomplete
- **Solution:**
Add NVMx power resource and remove _PS0/_PS3
Platform Affected:
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchRstPcieStorage.asl





64 Version 1.0.5 Details

Production Version Update

64.1 New Features

64.1.1 Feature 1

- **Description:**
Add detection time out for each of PCI root port
- **Solution:**
Created per-port policy for DetectTimeout
Platform Affected:
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

64.2 Fixed Bugs

64.2.1 Bug 1

- **Description:**
Incorrectly resetting Cycle Router's EGCR.TSCAS
- **Solution:**
Added function which checks whether any of the remapped drives does not use Msix interrupts.
Platform Affected:
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

64.2.2 Bug 2

- **Description:**
Incorrect register XHCI DBC DBCCTL offset setting
- **Solution:**
Corrected programming to 0x8760
Platform Affected:



All SKL/KBL

- **Affected Files:**

KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h

64.2.3 Bug 3

- **Description:**

mPchResetProtocol protocol installation incorrect

- **Solution:**

Updated level of indirection for pointer in question

Platform Affected:

All SKL/KBL

- **Affected Files:**

KabylakeSiliconPkg/Pch/Reset/RuntimeDxe/PchReset.c



65 Version 1.0.4 Details

Production Version Update

65.1 New Features

65.1.1 Feature 1

- **Description:**
BIOS assigns B0:D27 PCIe to ITSS_PIR6
- **Solution:**
Programming of PIR6 (INTx->PIRQy) interrupt register for D27 was missing from RC.

NOTE: This was not an issue as BIOS uses HW default interrupt routing for this device. The change is added to Silincon Init Code it so that it is clear for users on how interrupt configuration is applied.

Platform Affected:

All SKL/KBL

- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInterruptAssign.c

65.2 Fixed Bugs

65.2.1 Bug 1

- **Description:**
chXhciLegacySmiEnGet() & PchXhciLegacySmiEnSet() points to PCI Base & not MMIO Base in PchXhciLib.c file
- **Solution:**
Fixed pointers
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiDxeSmmPchXhciLib/PchXhciLib.c

65.2.2 Bug 2

- **Description:**



PCIe3 not performing link equalization. Common Clock Config bit will be set before PCIe Gen3 training is attempted. Without this bit training is less stable and when silicon reaches high temperature, Gen3 Eq might fail

- **Solution:**
Correct Common Clock Config bit
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/Pch/Library/Private/PeiDxeSmmPchPciExpressHelpersLib/PchPciExpressHelpersLibrary.c
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchRootPorts.c

65.2.3 Bug 3

- **Description:**
XHCI XHCC settings are lost after S5 is triggered from Win7
- **Solution:**
To work around this BIOS needs to set XHCC1, XHCC2 and XHCCLKGTEN registers again.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchUsb.c

65.2.4 Bug 4

- **Description:**
Fixing comment in PchInfoLib
- **Solution:**
Changed RST mode supported by platform to RST mode supported by silicon in GetSupportedRstMode function comment
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/Library/PchInfoLib.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c

65.2.5 Bug 5

- **Description:**
Intel RST and System Acceleration with Intel Optane Technology Mode NOT available to select for SATA Mode
- **Solution:**



Added enumeration which enumerates supported RST modes including the new Optane mode.

Platform Affected:

All SKL/KBL

- **Affected Files:**

/KabyLakeSiliconPkg/Pch/Include/Library/PchInfoLib.h

/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c

65.2.6 Bug 6

- **Description:**

Incorrect usage of assert_efi_error

- **Solution:**

Fix to use ASSERT.

Platform Affected:

All SKL/KBL

- **Affected Files:**

/KabyLakeSiliconPkg/Pch/Library/Private/PeiPchInitLib/PchInterruptAssign.c



66 Version 1.0.3 Details

Production Version Update

66.1 New Features

66.1.1 Feature 1

- **Description:**
Setup option to disable PMC patch
- **Solution:**
Additional test menu option to skip sending PMC MTPMC message
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakePlatSamplePkg/FspWrapper/Library/PeiFspPolicyInitLib/PeiFspPchPolicyInitLib.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

66.2 Fixed Bugs

66.2.1 Bug 1

- **Description:**
Incorrect pointer casting cause system hang
- **Solution:**
Fixed InstallPchReset() return pointer
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Reset/RuntimeDxe/PchReset.c

66.2.2 Bug 2

- **Description:**
Restrict PCI lanes Tx/Rx until reference clock is available
- **Solution:**
Provided lower bound of Trefclkon calculation
- **Platform Affected:**



All SKL/KBL

- **Affected Files:**
/KabylakeSiliconPkg/Include/PcieRegs.h

66.2.3 Bug 3

- **Description:**
SLP_S0B doesn't assert with NVM Remapping enabled
- **Solution:**
Added SATA's GCR bit[28] setting for every Cycle Router in NVM remapping flow.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

66.2.4 Bug 4

- **Description:**
0x0002 BIOS Hang
- **Solution:**
Fix NVM-R W/A
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

66.2.5 Bug 5

- **Description:**
Cannot enable serial logs when FSP-T is skipped and FSP-M is used
- **Solution:**
Updated serial log configuration
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/SerialPortLib/SerialPortLib.c
/KabylakeSiliconPkg/Pch/Library/SecPchLib/SecPchLib.c
/KabylakeSiliconPkg/Pch/Library/SecPchLib/SecPchLib.inf



67 Version 1.0.2 Details

Production Version Update

67.1 New Features

67.1.1 Feature 1

- **Description:**
DC Wander bit adjusted based on the DMI links strapped to AC/DC coupling
- **Solution:**
Move programming for L1 sub to the BIOS code instead of Chipsetinit.bin
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsFia.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsHsio.h

67.1.2 Feature 2

- **Description:**
Provide a platform hook to enable DspModule
- **Solution:**
Moved implementation to Platform Pkg
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchHdaAcpi.c
/KabylakeSiliconPkg/SiNvsInternalOnly/PchNvs.aht

67.1.3 Feature 3

- **Description:**
Request to have files with defines having *.h extension
- **Solution:**
Moved defines to *.h files
- **Platform Affected:**



All SKL/KBL

- **Affected Files:**

- /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioAcpiDefines.h
 - /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioDefine.asl
 - /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
 - /KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchAcpiTables.inf

67.1.4 Feature 4

67.1.5 Feature 3

- **Description:**

- **Solution:**

- **Platform Affected:**

- All SKL/KBL

- **Affected Files:**

67.2 Fixed Bugs

67.2.1 Bug 1

- **Description:**

- SLP_S0 is active in Idle Display ON with Voltage Margining disabled

- **Solution:**

- Updated PM Init to account for VM disabled configurations.

- Platform Affected:**

- All SKL/KBL

- **Affected Files:**

- /KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
 - /KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c

67.2.2 Bug 2

- **Description:**

- UDK debugger not working once under BDS phase

- **Solution:**



Fixed interrupt source override.

Platform Affected:

All SKL/KBL

- **Affected Files:**
/KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.c

67.2.3 Bug 3

- **Description:**
TCO_STS bit does not cleared as expected
- **Solution:**
Added special handling for TCO_STS bit.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchxSmmHelpers.c
/KabylakeSiliconPkg/SystemAgent/Salnit/Dxe/IgdOpRegion.c

67.2.4 Bug 4

- **Description:**
SLP_S0 is active in Idle Display ON with Voltage Margining disabled
 - **Solution:**
- Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c



68 Version 1.0.1 Details

Production Version Update

68.1 New Features

68.1.1 Feature 1

- **Description:**
Add support for LPC DID uSFF SKU A155 QMU185
- **Solution:**
Update configuration files
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

68.1.2 Feature 2

- **Description:**
Add a banner showing SYSTEM REBOOT in the debug log
- **Solution:**
Inserted banner in the debug log right before BIOS initiates a CF9 reset
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c

68.1.3 Feature 3

- **Description:**
Add support for Stony Beach remapping
- **Solution:**
Added SATA.EGCR programming to mask BAR0 address bit[14]
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

68.1.4 Feature 4

- **Description:**
New optimizations for SataTestMode
- **Solution:**
Updated routine optimizations
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsSata.h

68.1.5 Feature 5

- **Description:**
MCFG MMIO config space unclear in the memory map table
- **Solution:**
Reformatted memory map table for clarity.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Reset/RuntimeDxe/PchReset.c
/KabylakeSiliconPkg/Pch/Spi/RuntimeDxe/PchSpi.c

68.2 Fixed Bugs

68.2.1 Bug 1

- **Description:**
FSP should not reset the platform but instead it should return from the API with proper "FSP_STATUS_RESET_REQUIRED" return
- **Solution:**
Modify FSP code to return reset request
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/IntelFsp2Pkg/Include/FspEas/FspApi.h
/IntelFsp2WrapperPkg/FspmWrapperPeim/FspmWrapperPeim.c
/IntelFsp2WrapperPkg/FspsWrapperPeim/FspsWrapperPeim.c
/IntelFsp2WrapperPkg/FspWrapperNotifyDxe/FspWrapperNotifyDxe.c
/IntelFsp2WrapperPkg/FspWrapperNotifyDxe/FspWrapperNotifyDxe.inf
/IntelFsp2WrapperPkg/Include/Library/FspWrapperPlatformLib.h
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLibFsp.inf



68.2.2 Bug 2

- **Description:**
SLP_S0B doesn't assert
- **Solution:**
Enable NVM-Remapping
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsSata.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

68.2.3 Bug 3

- **Description:**
GpioSetAttributes returns failure and asserts when trying to set PadConfiguration
- **Solution:**
Exclude NMI capabilities from asserting with GpioSetAttributes
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLib.c

68.2.4 Bug 4

- **Description:**
Incorrect BIOS reset values
- **Solution:**
Replaced Cold boot 0xCF9 write 0x06 with 0xCF9 write 0x0E and Warm boot 0xCF9 write 0x04 with 0xCF9 write 0x06
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Me/HeciInit/Dxe/MeInit.c
/KabylakeSiliconPkg/Me/Library/DxeMeLib/MeDxeLibInternals.h
/KabylakeSiliconPkg/Pch/Library/BaseResetSystemLib/BaseResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/PeiPchResetLib/PchReset.c
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c



68.2.5 Bug 5

- **Description:**
Cannot perform reset after re-enable ME State
- **Solution:**
Fixed ResetData and DataSize while reset type is EfiResetPlatformSpecific
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Me/Include/Library/PeiMeLib.h
/KabylakeSiliconPkg/Me/Library/PeiMeLib/MePeiLibInternals.h
/KabylakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.c
/KabylakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.inf
/KabylakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSystemLib.inf
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c
/KabylakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.inf

68.2.6 Bug 6

- **Description:**
PM1_CNT shutdown asserts in GbeWolWorkaround
- **Solution:**
Added support between MAC and PHY for interface settings.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchLanSxSmm.c

68.2.7 Bug 7

- **Description:**
PCH should add ResetSystemLib instance
- **Solution:**
Added ResetSystemLib instance for SEC/PEI/DXE phase.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeSiliconPkg/Me/HeciInit/Dxe/HeciInit.inf
/KabylakeSiliconPkg/Me/HeciInit/Dxe/MeInit.c
/KabylakeSiliconPkg/Me/Library/DxeMeLib/DxeMeLib.inf
/KabylakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.c



```
/KabyLakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.h
/KabyLakeSiliconPkg/Me/MePlatformReset/RuntimeDxe/MePlatformReset.inf
/KabyLakeSiliconPkg/Pch/Include/Protocol/PchReset.h
/KabyLakeSiliconPkg/Pch/Library/BasePchResetCommonLib/BasePchResetCommonLib
.inf
/KabyLakeSiliconPkg/Pch/Library/BasePchResetCommonLib/PchResetCommon.c
/KabyLakeSiliconPkg/Pch/Library/BaseResetSystemLib/BaseResetSystemLib.c
/KabyLakeSiliconPkg/Pch/Library/BaseResetSystemLib/BaseResetSystemLib.inf
/KabyLakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSyste
mLib.c
/KabyLakeSiliconPkg/Pch/Library/DxeRuntimeResetSystemLib/DxeRuntimeResetSyste
mLib.inf
/KabyLakeSiliconPkg/Pch/Library/PeiPchResetLib/PchReset.c
/KabyLakeSiliconPkg/Pch/Library/PeiPchResetLib/PeiPchResetLib.inf
/KabyLakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.c
/KabyLakeSiliconPkg/Pch/Library/PeiResetSystemLib/PeiResetSystemLib.inf
/KabyLakeSiliconPkg/Pch/Reset/RuntimeDxe/PchReset.c
/KabyLakeSiliconPkg/Pch/Reset/RuntimeDxe/PchReset.h
/KabyLakeSiliconPkg/Pch/Reset/RuntimeDxe/PchResetRuntime.inf
/KabyLakeSiliconPkg/SiPkg.dec
/KabyLakeSiliconPkg/SiPkgCommonLib.dsc
/KabyLakeSiliconPkg/SiPkgDxeLib.dsc
/KabyLakeSiliconPkg/SiPkgPeiLib.dsc
```

68.2.8 Bug 9

- **Description:**
LTR override gets re-enforced after device hot-unplugged
- **Solution:**
Hot plug support was improved to allow re-enabling LTR override.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Smm/PchPcieSmm.c

68.2.9 Bug 10

- **Description:**
Determine MMIO resource issue on Hybrid Graphics with KBL Reference Code.
- **Solution:**
Pcie RP disabling moved to pre-mem, together with policy that controls it.



- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspBinPkg/Fsp.bsf
/KabylakeFspBinPkg/Include/FspmUpd.h
/KabylakeFspBinPkg/Include/FspsUpd.h
/KabylakeFspPkg/Include/FspmUpd.h
/KabylakeFspPkg/Include/FspsUpd.h
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiPchPolicyUpdatePreMem.c
/KabylakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiPolicyUpdatePreMemLib.inf
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsPcie.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPreMemPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.inf
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPreMemPolicyLib.c

68.2.10 Bug 11

- **Description:**
HTIM Register not configured with optimal value
- **Solution:**
Updated SMBUS interface HTIM register with optimal value from SPT
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Library/SecPchLib/SecPchLib.c



69 Version 1.0.0 Details

Production Version Update

69.1 New Features

No new features added

69.2 Fixed Bugs

No new bug fixes added



70 Version 0.9.1 Details

Production Version Update

70.1 New Features

70.1.1 Feature 1

- **Description:**
Added support for SLP_S0 LED on TYPE C board
- **Solution:**
Create SLP_S0# Voltage Margining enable/disable in setup
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c



71 Version 0.9.0 Details

Production Version Update

71.1 New Features

71.1.1 Feature 1

- **Description:**
Updated mPhy settings and added new rootport setup questions.
- **Solution:**
N/A
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.fdf
/KabylakeSiliconPkg/Pch/Include/Protocol/PchInfo.h
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.c

71.2 Fixed Bugs

71.2.1 Bug 1

- **Description:**
Wake from S3/S4 is not working through TBT dock
- **Solution:**
PCIEXP_WAKE_DIS bit is not cleared by OS, BIOS will clear this bit in case of Native PCIe disable while going into sleep.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsPmc.h



72 Version 0.8.1 Details

Production Version Update

72.1 New Features

72.1.1 Feature 2

- **Description:**
Remove SLP_S0 with display ON feature
- **Solution:**
Set XTALSDQDIS=0 for HDA D0 outside CS state.
- **Platform Affected:**
All SKL/KBL
Affected Files:
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl

72.1.2 Feature 3

- **Description:**
Suppress duplicate notify events in FSP wrapper mode
- **Solution:**
use FSP_WRAPPER_FLAG to ignore the secondary notify event
- **Platform Affected:**
All SKL/KBL
Affected Files:
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.h
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.c
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.inf
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxeFsp.inf
/KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitFsp.c

72.2 Fixed Bugs

72.2.1 Bug 2

- **Description:**
'Mutux not acquired' during ACPI DSDT Method Semantic tests
- **Solution:**
Fixed condition logic
- **Platform Affected:**



Version 3.8.0 Details

All SKL/KBL

- **Affected Files:**

/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchRstPcieStorage.asl

73 Version 0.8.0 Details

Production Version Update

73.1 New Features

73.1.1 Feature 1

- **Description:**
Increase dynamic support required for Optane/RST features.
- **Solution:**
Modify policies from PciPlatform
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/SataConfig.h
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsSata.h
/KabyLakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
/KabyLakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

73.1.2 Feature 2

- **Description:**
New RST Menu support for Optane
- **Solution:**
Add storage device detection to PEI phase that is passed to BIOS setup
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeFspPkg/KabyLakeFspPkg.dsc
/KabyLakeSiliconPkg/Pch/Include/Library/PchPcieRpLib.h
/KabyLakeSiliconPkg/Pch/Include/PchPcieStorageDetectHob.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchPcieRpLib/PchPcieRpLib.c
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.inf
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c
/KabyLakeSiliconPkg/SiPkg.dec
/KabyLakeSiliconPkg/SiPkgCommonLib.dsc

73.1.3 Feature 3

- **Description:**
Add password support for VTIO sideband access
- **Solution:**



Disable controller sideband access

- **Platform Affected:**

All SKL/KBL

- **Affected Files:**

/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Me/HeciInit/Dxe/EndOfPost.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/P2sbConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

73.2 Fixed Bugs

73.2.1 Bug 1

- **Description:**

System shutdown ~1min after S3 exit when warm reset overclocking is enable

- **Solution:**

Disable WDT on S3. S4 now matches S5 flow

- **Platform Affected:**

All SKL/KBL

- **Affected Files:**

/KabylakeSiliconPkg/Pch/Wdt/Dxe/WdtDxe.c



74 Version 0.7.3 Details

Production Version Update

74.1 New Features

74.1.1 Feature 1

- **Description:**
Add support for new Halo SKU's
- **Solution:**
Add New Kabylake PCH-LP LPC DIDs
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

74.1.2 Feature 2

- **Description:**
Add Optane support for KBL
- **Solution:**
Add new menu for Optane options
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Library/PchInfoLib.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

74.1.3 Feature 3

- **Description:**
KBL Allow SLP_S0 with display ON
- **Solution:**
Removed VM enable for HDA disabled from PEI
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl



74.1.4 Feature 4

- **Description:**
Add support for new DT SKU's
- **Solution:**
- Add New Kabylake PCH-H LPC DIDs
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

74.1.5 Feature 5

- **Description:**
Optimize BIOS setting for cAVS SRAM
- **Solution:**
Set SRAM Retention Mode Idle Wait to 256 XTAL oscillator clocks (PDDC.SRMIW = 110b)
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsHda.h

74.1.6 Feature 6

- **Description:**
Update ACPI LPIT to use SLP_S0# residency counter with BIOS switch option to use Package C10 residency counter
- **Solution:**
Added Setup option to switch b/w C10 and SLP So residency counter and changing the deepest State counter based on the setup option
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/ClientCommonPkg/Include/LowPowerIdleTable.h
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsPmc.h

74.1.7 Feature 7

- **Description:**
Add Intel Smart Sound Technology ISVs
- **Solution:**



Added new Audio FW IPs (for audio DSP pre-processing and post-processing)

- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h

74.2 Fixed Bugs

74.2.1 Bug 1

- **Description:**
SLP-S0 is not asserting in KBL Halo Boards.
- **Solution:**
Added high VCCIO VR ramp up time during CS exit
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h

74.2.2 Bug 2

- **Description:**
Memory Init Status always set to 0 = SUCCESS for DID message
- **Solution:**
Changed the setup defaults
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeFspPkg/KabyLakeFspPkg.dsc
/KabyLakeSiliconPkg/Me/Include/ConfigBlock/MePeiConfig.h

74.2.3 Bug 3

- **Description:**
Machine hangs at post code 0x0004 in SecCarInit on resme S3
- **Solution:**
Updated in the SMM handler
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Smm/PchXhciSxSmm.c



/KabyLakeSiliconPkg/Me/Include/ConfigBlock/MePeiConfig.h

74.2.4 Bug 4

- **Description:**
UART DEV ID CSPEC mismatch
- **Solution:**
Update UART DEV ID
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsSerialIo.h

74.2.5 Bug 5

- **Description:**
CM236 is not recognized as premium SKU
- **Solution:**
Removed CM236 from list of SKUs with no RAID available
- **Platform Affected:**
CM236
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c



75 Version 0.7.2 Details

Production Version Update

75.1 New Features

75.1.1 Feature 1

- **Description:**
Add eMMC tuning flow to support driver strength selection
- **Solution:**
Updated HS400 initialization flow to reflect re-tuning need when driver strength parameter value changes.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/ConfigBlock/ScsConfig.h
KabylakeSiliconPkg/Pch/Include/Protocol/PchEmmcTuning.h
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchScs.c

75.1.2 Feature 2

- **Description:**
New SPTLP eMMC HS400 DLL tuning 40-ohm driver strength default
- **Solution:**
Changed default eMMC Driver Strength value to 40ohm.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/ConfigBlock/ScsConfig.h
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchScs.c

75.1.3 Feature 3

- **Description:**
Added support for SG/HG for KBL-Y
- **Solution:**
Support for HG/SG is available on KBL-U/DT/HALO need to extent the support for KBL-Y.
- **Platform Affected:**
All SKL/KBL



- **Affected Files:**
KabylakeSiliconPkg/SystemAgent/AcpiTables/SwitchableGraphics/Pch/SgAcpiTablesPch.inf
KabylakeSiliconPkg/SystemAgent/AcpiTables/SwitchableGraphics/Pch/SgDgpuPch.asl
KabylakeSiliconPkg/SystemAgent/AcpiTables/SwitchableGraphics/Pch/SgSsdtPch.asl
KabylakeSiliconPkg/SystemAgent/AcpiTables/SwitchableGraphics/Pch/SgUlt.asl
KabylakeSiliconPkg/SystemAgent/AcpiTables/SwitchableGraphics/Pch/SgUlx.asl
KabylakeSiliconPkg/SystemAgent/SalNit/Dxe/SwitchableGraphicsInit.c
KabylakeSiliconPkg/SystemAgent/SalNit/Dxe/SwitchableGraphicsInit.h

75.1.4 Feature 4

- **Description:**
Add Kabylake PCH-LP LPC DIDs
- **Solution:**
Add support for new device ID that were added for KBL PCH LP skews
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

75.2 Fixed Bugs

75.2.1 Bug 1

- **Description:**
ASL Warning 3115 messages on KBL Project
- **Solution:**
Audited and fixed ASL data types
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchRstPcieStorage.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSata.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXdci.asl
KabylakeSiliconPkg/SystemAgent/AcpiTables/PegSsdt/PegOnOff.asl



75.2.2 Bug 2

- **Description:**
Policy data should be preserved for both Pei and Dxe
- **Solution:**
Built a policy HOB
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.h
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/CpuInitDxe.inf
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpCommon.c
KabylakeSiliconPkg/Cpu/CpuInit/Dxe/MpService.c
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.h
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.c
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.inf
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxeFsp.inf
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c
KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.c
KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.inf
KabylakeSiliconPkg/Pch/PchInit/Smm/PchPcieSmm.c
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/loTrap.c
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmiDispatcher.inf
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmm.h
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmmCore.c
KabylakeSiliconPkg/Pch/Wdt/Dxe/WdtDxe.c
KabylakeSiliconPkg/Pch/Wdt/Dxe/WdtDxe.inf
KabylakeSiliconPkg/SilInit/Pei/SilInit.c
KabylakeSiliconPkg/SilInit/Pei/SilInit.h
KabylakeSiliconPkg/SilInit/Pei/SilInit.inf
KabylakeSiliconPkg/SiPkg.dec
KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/GraphicsInit.c
KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/IgdOpRegion.c
KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/SaInit.inf
KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/SaInitFsp.inf
KabylakeSiliconPkg/SystemAgent/SaInit/Dxe/VTd.h
KabylakeSiliconPkg/SystemAgent/SmmAccess/Dxe/SmmAccess.inf
KabylakeSiliconPkg/SystemAgent/SmmAccess/Dxe/SmmAccessDriver.c
KabylakeSiliconPkg/SystemAgent/SmmAccess/Dxe/SmmAccessDriver.h

75.2.3 Bug 3

- **Description:**



- Failed to detect valid PCIe dev/func numbers on KBL
- **Solution:**
Corrected KBL dev/func numbers
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchPcieRpLib/PchPcieRpLib.c

75.2.4 Bug 4

- **Description:**
Ctrl+P MEBx prompt is not seen during platform boot.
- **Solution:**
Correct the HOB address which gets in DXE for ME/AMT policies.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Me/Library/DxeAmtLib/AmtPolicyDxeLib.c
KabylakeSiliconPkg/Me/Library/DxeMeLib/MePolicyDxeLib.c

75.2.5 Bug 5

- **Description:**
RC 0.7 will hang if set PcdS3Enable|FALSE
- **Solution:**
Cleared SWSMI STS bit when SmmControl triggers an SMI
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/PchSmiDispatcher/Smm/PchSmmCore.c



76 Version 0.7.1 Details

Production Version Update

76.1 New Features

76.1.1 Feature 1

- **Description:**
Add support for a new KBL-H SKUs
- **Solution:**
Add support for a new KBL-H SKUs two new skus
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
/KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c

76.1.2 Feature 2

- **Description:**
Align PCH IO APIC with customer requests
- **Solution:**
Update PCH policy for IO APIC
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/IOApicConfig.h

76.1.3 Feature 3

- **Description:**
Add Added new 3rd party IP support for Sound Research
- **Solution:**
Add Sound Research GUID for IntelSST config
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h



76.2 Fixed Bugs

76.2.1 Bug 1

- **Description:**
BSOD 9F Observed with ACPI.sys during S3 cycling
- **Solution:**
GPIO ASL lib incorrect macro definition caused CGLS() method not clear GPE_STS correctly
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioLib.asl

76.2.2 Bug 2

- **Description:**
DCI Enable not working
- **Solution:**
Update PEI policy
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/ConfigBlock/DciConfig.h



77 Version 0.7.0 Details

Production Version Update

77.1 New Features

77.1.1 Feature 1

- **Description:**
De-feature PEI_CACHE_PPI
- **Solution:**
Use MtrrLib from UefiCpuPkg and stop producing PEI_CACHE_PPI
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.fdf
/KabylakeSiliconPkg/Cpu/Include/Ppi/Cache.h
/KabylakeSiliconPkg/KabylakeSiliconPkg.dsc

77.1.2 Feature 2

- **Description:**
Support RVP3 specific features through library
- **Solution:**
Create library instance for RVP3
- **Platform Affected:**
RVP3 SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/Library/PchPolicyLib.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.inf
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/Rvp3PolicyLib.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/Rvp3PreMemPolicyLib.c

77.1.3 Feature 3

- **Description:**
De-feature PTTSwitch.
- **Solution:**
Remove all references to PTTSwitch
- **Platform Affected:**
All SKL/KBL



- **Affected Files:**
 - /KabylakeFspBinPkg/Fsp.bsf
 - /KabylakeFspBinPkg/Include/FspmUpd.h
 - /KabylakeFspBinPkg/Include/FspUpd.h
 - /KabylakeFspPkg/Include/FspmUpd.h
 - /KabylakeFspPkg/Include/FspUpd.h
 - /KabylakeFspPkg/KabylakeFspPkg.dsc
 - /KabylakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiMePolicyUpdatePreMem.c
 - /KabylakeSiliconPkg/Me/AcpiTables/MeSsdT/MeSsdT.asl
 - /KabylakeSiliconPkg/Me/Include/ConfigBlock/MePeiConfig.h
 - /KabylakeSiliconPkg/Me/Include/Protocol/MeGlobalNvsArea.h
 - /KabylakeSiliconPkg/Me/Library/PeiMePolicyLib/PeiMePolicyLib.c
 - /KabylakeSiliconPkg/Me/Ptt/Smm/Ptt.asl

77.1.4 Feature 4

- **Description:**

New PCH-H A0 stepping support needs to be introduced into Kabylake BIOS.
- **Solution:**

Add Kabylake PCH-H A0 stepping
- **Platform Affected:**

All SKL/KBL
- **Affected Files:**
 - /KabylakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h
 - /KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoLib.c
 - /KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchInfoLib/PchInfoStrLib.c
 - /KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchPcieRpLib/PchPcieRpLib.c
 - /KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c
 - /KabylakeSiliconPkg/Pch/PchInit/Smm/PchPcieSmm.c

77.1.5 Feature 5

- **Description:**

PostCodes to be added for individual components - PCH-ME
- **Solution:**

Update effected files
- **Platform Affected:**

All SKL/KBL
- **Affected Files:**
 - /KabylakeSiliconPkg/Me/ActiveManagement/AlertStandardFormat/Dxe/AlertStandardFormatDxe.c
 - /KabylakeSiliconPkg/Me/BiosExtensionLoader/Dxe/BiosExtensionLoader.c
 - /KabylakeSiliconPkg/Me/Library/DxeMeLib/DxeMeLib.inf
 - /KabylakeSiliconPkg/Me/Library/DxeMeLib/HeciMsgDxeLib.c



/KabyLakeSiliconPkg/Me/Library/DxeMeLib/MeDxeLibInternals.h
/KabyLakeSiliconPkg/Me/Library/PeiMeLib/HeciMsgPeiLib.c
/KabyLakeSiliconPkg/Me/Library/PeiMeLib/PeiMeLib.inf

77.1.6 Feature 7

- **Description:**
Increase PeiDxeSmmGpioLib pad support to 32
- **Solution:**
Update effected files
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioLib.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/GpioLibObjects.asl
/KabyLakeSiliconPkg/Pch/Include/Library/GpioLib.h
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsGpio.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioInit.c
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLib.c
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLibrary.h
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioNativeLib.c
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/PchSkLgpioData.c

77.1.7 Feature 8

- **Description:**
Updated NVM Remapping flow in BIOS to support new PCIe controller on KBP-H.
- **Solution:**
Update effected files
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

77.2 Fixed Bugs

77.2.1 Bug 1

- **Description:**
DevSlp PadRstCfg register initialization failure
- **Solution:**
Update GpioHandleSataDevSlpPad() and GpioHandleGSpiCSBPad() to correctly configure PadRst setting for DevSlp pin case.
- **Platform Affected:**



All SKL/KBL

- **Affected Files:**

/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioInit.c

77.2.2 Bug 2

- **Description:**

Performance settings not optimized for newer system configuration

- **Solution:**

Disable TDC by default

- **Platform Affected:**

All SKL/KBL

- **Affected Files:**

/KabyLakeSiliconPkg/Cpu/Include/ConfigBlock/CpuPowerMgmtVrConfig.h

/KabyLakeSiliconPkg/Cpu/Library/PeiCpuPolicyLib/PeiCpuPolicyLib.c

77.2.3 Bug 3

- **Description:**

PCR value incorrectly set to zero after S3 resume

- **Solution:**

Move the PTT return code into the PTT device library

- **Platform Affected:**

All SKL/KBL with FSP

- **Affected Files:**

/KabyLakeSiliconPkg/Me/Include/Protocol/MeGlobalNvsArea.h

/KabyLakeSiliconPkg/Me/Library/PeiDxePttPtpLib/PeiDxePttPtpLib.c

77.2.4 Bug 4

- **Description:**

RVP11 hangs at 0xB00 with debug build

- **Solution:**

Added PCH-H mobile SKU to SKL-PCH check

- **Platform Affected:**

RVP11 SKL/KBL

- **Affected Files:**

/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsLpc.h

77.2.5 Bug 5

- **Description:**

XDCI_DSM return integer for “unsupported UUID” should be a buffer pointer.

- **Solution:**



- Update XDCI _DSM
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Me/Library/DxeAmtLib/AmtPolicyDxeLib.c
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHeci.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchIsh.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSata.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSeriallo.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/usbssbd.asl
/KabyLakeSiliconPkg/SystemAgent/AcpiTables/HostBus.asl

77.2.6 Bug 6

- **Description:**
System can not enter to SLP_S0
- **Solution:**
Updated method responsible for disabling ISH in PSF
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Library/PeiDxeSmmPchSerialloLib/PeiDxeSmmPchSerialloLib.c

77.2.7 Bug 7

- **Description:**
Properly handle NRMO and MSL register for RST disable case
- **Solution:**
Program NRMO to 0x00F and MSL to 0x0 for the RST disable case.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

77.2.8 Bug 8

- **Description:**
Update SKL Audio PLL setting
- **Solution:**



Version 3.8.0 Details

Updated register value: APLLP1.DCOTC = 1Eh

- **Platform Affected:**

All SKL/KBL

Affected Files:

/KabylakeSiliconPkg/Pch/Include/Register/PchRegsHda.h



78 Version 0.6.1 Details

Production Version Update

78.1 New Features

78.1.1 Feature 1

- **Description:**
Add enable/disable option in the SKL BIOS for Smart Amp
- **Solution:**
Add Smart Amp support in HDAS _DSM method
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h

78.1.2 Feature 2

- **Description:**
Convert PSF implementation into Library
- **Solution:**
Provide necessary API and change all PSF accesses to use it
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeFspPkg/KabylakeFspPkg.dsc
KabylakeSiliconPkg/Me/Library/PeiDxeMeChipsetLib/PeiDxeMeChipsetLib.c
KabylakeSiliconPkg/Me/Library/PeiDxeMeChipsetLib/PeiDxeMeChipsetLib.inf
KabylakeSiliconPkg/Pch/Include/Library/PchPsLib.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPsf.h
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchPsLib/PchPsLib.c
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchPsLib/PeiDxeSmmPchPsLib.inf
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchSerialIoLib/PeiDxeSmmPchSerialIoLib.c
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmPchSerialIoLib/PeiDxeSmmPchSerialIoLib.inf
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmTraceHubInitLib/PeiDxeSmmTraceHubInitLib.c
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmTraceHubInitLib/PeiDxeSmmTraceHubInitLib.inf



KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInit.h
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxe.inf
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitDxeFsp.inf
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchInitUefi.c
KabylakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c
KabylakeSiliconPkg/SiPkg.dec
KabylakeSiliconPkg/SiPkgCommonLib.dsc

78.1.3 Feature 3

- **Description:**
Disable TCO watchdog timer by default and add option to enable
- **Solution:**
Add policy TcoTimerEnable.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeFspBinPkg/Fsp.bsf
KabylakeFspBinPkg/Include/FspUpd.h
KabylakeFspBinPkg/Include/FspUpd.h
KabylakeFspPkg/Include/FspUpd.h
KabylakeFspPkg/Include/FspUpd.h
KabylakeFspPkg/KabylakeFspPkg.dsc
KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
KabylakeSiliconPkg/Pch/Include/ConfigBlock/PmConfig.h
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

78.1.4 Feature 4

- **Description:**
Add operation frequency support for SMBUS
- **Solution:**
Add setting for thigh and tlow fields on HTIM register
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeSiliconPkg/Pch/Library/SecPchLib/SecPchLib.c

78.1.5 Feature 5

- **Description:**
Leverage the definition of PCH_SBI_PID in ASL



- **Solution:**
Include header files for register definition in ASL code

- **Platform Affected:**
All SKL/KBL

- **Affected Files:**

KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchHda.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchPcie.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchRstPcieStorage.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSata.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchScs.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl
KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/TraceHubDebug.asl
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPcie.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPcr.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsPmc.h
KabylakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
KabylakeSiliconPkg/Pch/Library/PeiDxeSmmGpioLib/GpioLibrary.h
KabylakeSiliconPkg/SystemAgent/AcpiTables/PegSsdt/PegOnOff.asl

78.2 Fixed Bugs

78.2.1 Bug 1

- **Description:**
Fix locate verb table issue in Config Block for PCH
- **Solution:**
Use pointer policy for VerbTable structure and PCIE device ASPM override structure
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
KabylakeFspBinPkg/Fsp.bsf
KabylakeFspBinPkg/Include/FspmUpd.h
KabylakeFspBinPkg/Include/FspsUpd.h
KabylakeFspBinPkg/Include/FsptUpd.h
KabylakeFspBinPkg/Include/FspUpd.h
KabylakeFspPkg/FspInit/Pei/FspInitPreMem.inf
KabylakeFspPkg/Include/BootLoaderPlatformData.h
KabylakeFspPkg/Include/FspmUpd.h
KabylakeFspPkg/Include/FspsUpd.h
KabylakeFspPkg/Include/FsptUpd.h
KabylakeFspPkg/Include/FspUpd.h



Version 3.8.0 Details

KabylakeFspPkg/KabylakeFspPkg.dsc
KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPolicyUpdateLib.inf
KabylakeSiliconPkg/Pch/Include/ConfigBlock/HdAudioConfig.h
KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
KabylakeSiliconPkg/Pch/Include/ConfigBlock/SataConfig.h
KabylakeSiliconPkg/Pch/Include/Ppi/PchHdaVerbTable.h
KabylakeSiliconPkg/Pch/Include/Ppi/PchHsioPtssTable.h
KabylakeSiliconPkg/Pch/Include/Ppi/PchPcieDeviceTable.h
KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c
KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.h
KabylakeSiliconPkg/SiPkg.dec



79 Version 0.6.0 Details

Production Version Update

79.1 New Features

79.1.1 Feature 1

- **Description:**
Policy setting request to disable CPM on PCIe root port
- **Solution:**
EnableCpm field was added to PCH Policy. By default it is enabled.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/PcieRpConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPolicyLib.c
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchPcieSmm.c

79.1.2 Feature 2

- **Description:**
UPD to configure SPD Write Disable bit
- **Solution:**
Add policy to not set SPD write disable
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspBinPkg/DualFsp/Include/FspUpdVpd.h
/KabylakeFspBinPkg/Fsp.bsf
/KabylakeFspBinPkg/Include/FspUpdVpd.h
/KabylakeFspPkg/Include/FspUpdVpd.h
/KabylakeFspPkg/Include/FspUpdVpdInternal.h
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/KabylakeFspPkg.fdf
/KabylakeFspPkg/Library/PeiPolicyUpdatePreMemLib/PeiPchPolicyUpdatePreMem.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SmbusConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPreMemPrintPolicy.c
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PeiPchPreMemPolicyLib.c

79.1.3 Feature 3

- **Description:**

- Static Clock Gating Enable (8254CGE) not set in FSP
- **Solution:**
Provide UPD wrapper for FSP regarding 8254CGE.
- **Platform Affected:**
All SKL/KBL SKUs
- **Affected Files:**
/KabylakeFspBinPkg/Fsp.bsf
/KabylakeFspBinPkg/Include/FspUpdVpd.h
/KabylakeFspPkg/Include/FspUpdVpd.h
/KabylakeFspPkg/Include/FspUpdVpdInternal.h
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/Library/PeiPolicyUpdateLib/PeiPchPolicyUpdate.c
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/IoApicConfig.h
/KabylakeSiliconPkg/Pch/Include/ConfigBlock/SmbusConfig.h
/KabylakeSiliconPkg/Pch/Library/PeiPchPolicyLib/PchPrintPolicy.c

79.1.4 Feature 4

- **Description:**
Added WWAN enable/disable option
- **Solution:**
Added WWAN enable/disable option
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeFspPkg/KabylakeFspPkg.dsc
/KabylakeFspPkg/KabylakeFspPkg.fdf

79.2 Fixed Bugs

79.2.1 Bug 1

- **Description:**
S4 TraceHub Out of resources.
- **Solution:**
Increase resources available for S4 TraceHub
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchAcpiTables.inf
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSmb.asl
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.c



79.2.2 Bug 2

- **Description:**
System throws BSOD ACPI_BIOS_ERROR while booting to windows when Aperture Size is set to 4096MB.
- **Solution:**
Added 64bits MMIO address support.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/AcpiTables/Dsdt/PchXhci.asl

79.2.3 Bug 3

- **Description:**
RAID 0 does not work when configured as PCIE 2x2
- **Solution:**
Corrected error in strap configuration reading
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchRstPcieStorage.c

79.2.4 Bug 4

- **Description:**
FSP not to set the ACCTRL bit for XHCI Device
- **Solution:**
Move XHCI lock to EndOfDxe
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/PchInit/Dxe/PchInit.c

79.2.5 Bug 5

- **Description:**
Extra D3 entry with D3HE set
- **Solution:**
Remove extra entry
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabyLakeSiliconPkg/Pch/Include/Register/PchRegsUsb.h
/KabyLakeSiliconPkg/Pch/PchInit/Smm/PchXhciSxSmm.c



79.2.6 Bug 6

- **Description:**
Update SMBUS ASL code to support CMI specification
- **Solution:**
SMBUS ASL does not comply with CMI spec permitting race condition between ASL code and driver.
- **Platform Affected:**
All SKL/KBL
- **Affected Files:**
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/Pch.asl
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchAcpiTables.inf
/KabylakeSiliconPkg/Pch/AcpiTables/Dsdt/PchSmb.asl
/KabylakeSiliconPkg/Pch/PchInit/Smm/PchInitSmm.c

79.3 Known Issues

None



80 Version 0.5.0 Details

Initial Release

80.1 New Features

None

80.2 Fixed Bugs

None

80.3 Known Issues

None