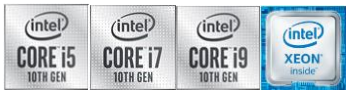
Production Release Qualification Report

Intel® Core™ i9 Processor series
Intel® Core™ i7 Processor series
Intel® Core™ i5 Processor series
Intel® Xeon® Processor series



14nm Technology in a LGA1200 Package
Q Step 20/16/12 MB Cache

Products included in this Production Release Qualification Report

Stepping	Product Name	S-SPEC	MM#	Core Freq	GT Freq
Q	8070104282134	RH6R	F999W41	4.1 GHz	1.2 GHz
Q	8070104282215	RH6U	F999W44	2 GHz	1.2 GHz
Q	8070104282327	RH6Y	F999W4A	2.9 GHz	1.2 GHz
Q	8070104282436	RH72	F999W4G	3.8 GHz	1.2 GHz
Q	8070104282718	RH78	F999W51	2.9 GHz	1.1 GHz
Q	8070104282719	RH79	F999W52	2.9 GHz	0 GHz
Q	8070104381006	RH7H	F999W5C	4.1 GHz	1.2 GHz
Q	8070104282515	RH8Y	F999WX5	1.9 GHz	1.2 GHz
Q	8070104282624	RH8Z	F999WXC	2.8 GHz	1.2 GHz
Q	8070104282844	RH91	F999WXM	3.7 GHz	1.2 GHz
Q	8070104378412	RH93	F999WXW	3.7 GHz	1.2 GHz
Q	8070104379111	RH94	F999WXZ	3.2 GHz	1.2 GHz
Q	8070104380809	RH95	F999WZ1	3.8 GHz	1.2 GHz
Q	8070104380910	RH96	F999WZF	3.4 GHz	1.2 GHz
Q	8070104429007	RH97	F999WZH	1.9 GHz	1.2 GHz

April 2020
Original Issue

INTEL CONFIDENTIAL

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1.0 INTRODUCTION

This report covers the data collected to fulfill Production Release Qualification (PRQ) requirements for the Intel® Core™ Processors and Intel® Xeon® Processors.

The Intel® Core™ Processors and Intel® Xeon® Processors have been validated against the PRQ Quality and Reliability Verification requirements set forth in the Intel® Product Qualification System for the use-conditions that Intel has determined to represent the target usage segment(s) for Desktop PC .

1.1 Product Description

The 10th Generation Intel® Core™ Processor and Intel® Xeon® Processor families introduce the first S-series 10-core processors delivering outstanding single-threaded and multi-threaded performance from the next generation 64-bit, multi-core architecture built on Intel's most up-to-date and optimized 14-nanometer process technology. These S-series processors are designed for a two-chip platform pairing with an Intel® 400 series chipset and offer thermal design power (TDP) options of 125W, 80W, 65W and 35W. The processor includes Integrated Display Engine, Processor Graphics, PCI Express ports, and an Integrated Memory Controller. The S-series processors are ideally suited for applications like gaming, content creation, virtual reality, transactional retail terminals, digital security systems, and health care.

2.0 QUALITY AND RELIABILITY VERIFICATION

The Intel Quality and Reliability Verification (QRV) Process starts by defining the correct requirements early in the product design. It involves comprehensive product design and technology development integration, implementation of robust and controlled manufacturing processes and systems, and ultimately leads to Quality and Reliability Verification testing on the finished product.

This report documents the product QRV testing results. During QRV testing Intel uses both standards-based and knowledge-based qualification strategies to insure that Intel products are shipped with the highest quality while considering cost and practicality of these requirements. Intel uses industry accepted standards such as JEDEC and internally developed stress methodologies so that the products conform to the product quality and reliability requirements.

QRV stress tests were conducted on units that have completed the full manufacturing flow. In all cases, a failure is defined as a failure to meet datasheet parameters as measured by the appropriate production and/or engineering tester. QRV results are summarized in the following section with supporting experimental results in the subsequent pages.

3.0 SUMMARY OF QUALIFICATION RESULTS

Intel® Core™ Processors and Intel® Xeon® Processors

3.1 Use Reliability

Active & Inactive Operation→	0-1 Year (8760 hrs)	0-3 Year (26280 hrs)	0-5 Year (43800 hrs)
	CUM % Fail	CUM % Fail	CUM % Fail
Goals	0.24%	1.2%	1.85%
Estimated	0.24% (274 FIT)	0.46% (175 FIT)	0.68% (155 FIT)

3.2 Outgoing Quality

Indicator	Goal	Results
Outgoing Quality Assurance	500 DPM	397 DPM

3.3 Qualification Summary

Stress	Spec #	Stress Condition	Results
ESD – Human Body Model	ANSI/ESDA/JEDEC JS-001	±1000 V	0/9 units
ESD – Charged Device Model	ANSI/ESDA/JEDEC JS-002	±250 V	0/9 units
ESD – Direct Pin Zap – Latch-up	N/A	±1000 V	0/9 units
ESD – Direct Pin Zap – Lock-up	N/A	±600 V	0/9 units
Latch-up – Vcc	JESD78	1.5x VCC max DC	0/9 units
Latch-up – I/O	JESD78	±100 mA	0/9 units

3.4 Operating Reliability

Stress	Spec #	Stress Condition	Readout 1	Readout 2	Readout 3
Infant Mortality Evaluation	JESD94	90°C, 1.50 V	3/2111 units @ 0.25 hrs	4/2108 units @ 2 hrs	10/2104 units @ 20 hrs
Extended Life Test	JESD94	90°C, 1.50 V	1/249 units @ 1 hr	1/248 units @ 20 hrs	1/247 units @ 100 hrs

3.5 Thermal Mechanical

Stress	Spec #	Stress Condition	Readout 1	Readout 2
Temperature Cycling	JESD22-A104	-55°C to 125°C (Condition B)	0/307 units @ 750 cyc	X
High Temperature Storage (Bake)	JESD22-A103	150°C (Condition B)	0/601 units @ 504 hrs	0/601 units @ 1008 hrs
Accelerated Moisture Resistance – Unbiased HAST	JESD22-A118	110°C / 85%RH (Condition B)	0/308 units @ 100 hrs	X

4.0 USE RELIABILITY ASSESSMENT METHODOLOGY

4.1 Overview

This section provides a basic explanation of Intel's use reliability assessment methodology.

Intel follows a consistent and robust methodology for validating our products and delivering them to the market. This process begins with Technology Certification and reaches completion after product qualification when we grant Production Release Qualification (PRQ). Technology Certification focuses on validation of the package and silicon building blocks for our products. During this phase, the focus is on identifying possible failure mechanisms and risks associated with the technology. Evaluations are performed on package test vehicles and circuit level test structures to drive changes to material selection and the overall silicon and assembly process flow. During this phase very detailed failure models are developed for potential mechanisms that might be observed on the product. Upon completion of Technology Certification each product is required to execute a detailed Product Qualification in order to achieve PRQ. The product qualification focuses on validating that the product quality & reliability performance matches the technology model or baseline. This includes targeted evaluations to assess numerous product specific targets and goals, examples include Electrical Overstress (EOS), time-zero quality, and reliability failure characteristics.

Reliability failure characteristics are a function of time and usage. A technology baseline for each failure mechanism is derived using failure-mechanism testing, also known as knowledge-based testing as described in JEDEC Standard JESD94. This testing uses specific stresses that accelerate known failure mechanisms. The acceleration factors and time dependent (TTF) parameters are derived by including targeted use based evaluations in addition to unique accelerated stress conditions. Each failure mechanism type has a unique failure characteristic as a function of time and acceleration relative to use conditions as shown in Figure 1.

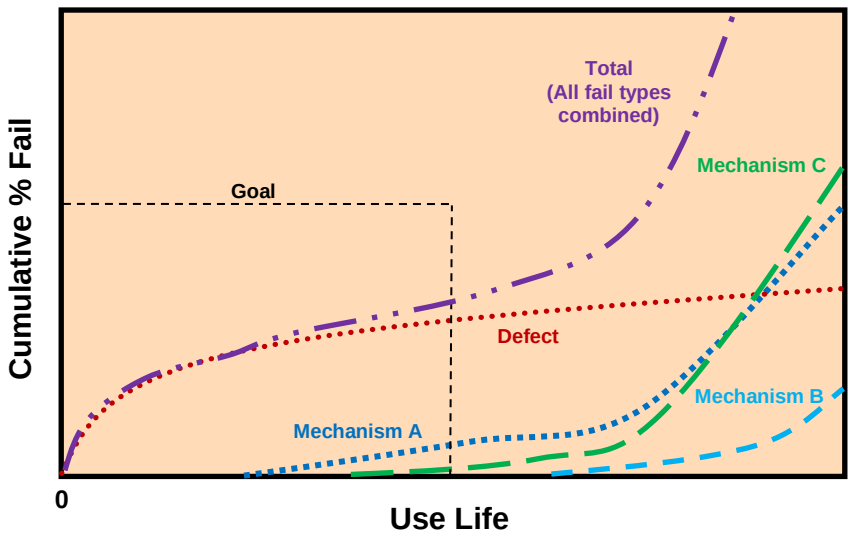


Figure 1: Example Failure Characteristics for Typical Defect and Intrinsic Failure Mechanisms.

As stated previously, this approach requires knowledge of the specific failure mechanisms and details on the target use conditions. Intel's long term product reliability is estimated by assessing each of the failure mechanisms at a reference use condition. The use condition consists of parameters associated with platform design, environmental conditions, and end-user behavior. The platform design parameters are outlined in the product datasheet. It is expected that the system meets all electrical and thermal requirements in the

datasheet since this bounds the operating region and defines the range of operating conditions assumed for the reliability assessment. For the environmental and end-user parameters, Intel has generated assumptions based on extensive data models of ambient conditions and component activity established by data acquisition projects under actual use environment. The technology is intended for use in non-condensing ambient temperature environments for civilian use.

NOTE: *The technology and civilian use products identified by this report are compliant to U.S. Department of Commerce export administration regulations (EAR) as defined by export control classification numbers (ECCN) 3A001 and 4A004 (where applicable).*

The reference use model can vary depending on targeted usage and market segment. For the products included in this quality and reliability report, the reference use assumptions noted in Table 1 (section 4.2) are associated with compliance to the datasheet requirements. The reference use conditions are Intel's best estimate of operation variables within the datasheet representing a time averaged scenario. Operation of a population of units at or below these reference use conditions on average will ensure the product will continue to meet Intel's quality and reliability goals.

4.2 Use Condition Definition

Use Condition Segment(s): Desktop PC

Product: Intel® Core™ Processors and Intel® Xeon® Processors

Category	Parameter	Value
Durations	Operating Time[3]	5 years (43,800 hrs)
Active Operation[1]	Time (%)	30
	Junction Temperature[4], T_j (°C)	60
Inactive Operation[2]	Time (%)	70
	Junction Temperature[4], T_j (°C)	35

Table 1: Product Reference Use Conditions[5]

Notes:

1. Active Operation means executing instructions.
2. Inactive Operation equates to time spent in idle and/or standby and/or off states.
3. Operating Time is the accumulated modeled time in years that a product spends in either active operation (i.e., executing instructions) or inactive operation (i.e., time spent in idle and/or standby states).
4. The Junction Temperature T_j (°C) is the estimated weighted average die temperature based on the operating conditions (Active or Inactive) and the component within a system at the target use condition.
5. Reference Use Condition values are intended to represent the integration over time of reliability-related conditions seen over the life of the product in typical use, and are not the same as Product Datasheet limits. Sustained exposure to extreme use environments that significantly deviate from the use environment described in Table 1 may affect long-term component reliability.

The reference use conditions described in Table 1 are used in the Intel® Core™ Processors and Intel® Xeon® Processors and are based on a Desktop PC . environment that comprehends various types of computing models and form factors (e.g., blade, tower, notebook). These reference use conditions are used in conjunction with the reliability models to assess the product's reliability during use in a system.

4.3 Use Reliability

Use Reliability[1] Results:

Active & Inactive Operation→	0-1 Year (8760 hrs)	0-3 Year (26280 hrs)	0-5 Year (43800 hrs)
	CUM % Fail	CUM % Fail	CUM % Fail
Goals[2]	0.24%	1.2%	1.85%
Estimated[3]	0.24% (274 FIT)	0.46% (175 FIT)	0.68% (155 FIT)

Notes:

1. "Use Reliability" is based on a statistically meaningful population of devices operating continuously for the "Active & Inactive Operation" duration. Failure rates are not constant, so they are not linear functions of time.
2. Intel's goals are based on a Knowledge Based Qualification Methodology (JESD94) and are intended to comprehend all relevant Extrinsic and Intrinsic fail mechanisms for all committed usage models and across manufacturing variation.
3. The estimated CUM % values represent projected component best estimates for a population of units, comprehending latent reliability defects and intrinsic failure mechanisms accelerated by the test evaluations documented in the PRQ report. The first year of continuous operation is dominated by latent reliability defect failures. Intel provides a translation of these CUM % estimates to FIT values for reference. By comparison, some customers may be familiar with a Standards Based Qualification (JESD47) which applies a Chi2 approach for Reliability Estimates and thus represents a different method.

The projected Average Failure Rate (FIT) for a given use time is provided to aid in system failure rate calculations. For system reliability budgets, the concept of failure rate budgets is valid for constant or time varying failure rates. It should be noted that Mean-Time-To-Failure or MTTF is computed from the reciprocal of failure rate as a reliability figure of merit. Generally MTTF and FIT are only valid for constant failure rates; however, Intel component failure rates are not constant nor are the resultant system failure rates.

5.0 OUTGOING ELECTRICAL QUALITY VALIDATION DPM

Description:
Outgoing Electrical Quality Validation measures the outgoing quality level by testing the electrical functionality and performance of the product before shipment. It is performed on material that has completed the standard production flow including assembly and electrical test.

Test Methodology:
The units are electrically tested using content and conditions which are comprehensive and specific to the product, which can include functional, structural and parametric content, as well as SKU-specific configuration testing.

Results:
Outgoing Electrical QV was completed on 20133 units across 58 production lots.

Outgoing Electrical Quality Validation

# of Lots	Product Name	Package	Results	DPM
58	8070104xxxxxx	LGA1200	8/20133[1]	397

Failure Summary:
1) 8 Functional fails

6.0 QUALIFICATION STRESS DETAILS

6.1 Electrostatic Discharge

Stress Description:

Electrostatic Discharge (ESD) testing is done to measure a device's sensitivity to electrostatic damage during handling. Human handling is simulated using the Human Body Model (HBM). This type of event occurs when a person transfers a charge from their body into a device. Intel uses ANSI/ESDA/JEDEC Joint Standard JS-001 in determining the appropriate HBM test conditions for each product. Mechanical handling is simulated using the Charged Device Model (CDM). This type of event occurs when a device accumulates charge during automated handling and is discharged to a low resistance, low inductance ground plane. Intel uses ANSI/ESDA/JEDEC Joint Standard JS-002 to establish the appropriate non-socketed CDM test conditions for each product.

Stress Conditions:

HBM ESD testing is done using an automated ESD tester. A 100pF capacitor is discharged into the device through a 1.5 kΩ resistor. The units are stressed to both polarities and are zapped once for each polarity. Pin combinations used are consistent with Tables 2A or 2B in ANSI/ESDA/JEDEC JS-001.

CDM ESD testing is done using an automated ESD tester. The device is charged via induction, and the device is discharged to a ground plane through the pin under test which is contacted with a robotic driven probe. Each pin under test is discharged one time when the device is charged positively with respect to ground and one time when the device is charged negatively with respect to ground.

Parts are functionally and parametrically tested after stress using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

HBM ESD (ANSI/ESDA/JEDEC JS-001)
Classification Level: Class 1C

Lot ID	Product Name	Package	Step	Stress Voltage	Results
J942007S	8070104xxxxxx	LGA1200	P	±1000 V	0/3
J942016S	8070104xxxxxx	LGA1200	P	±1000 V	0/3
J934007S	8070104xxxxxx	LGA1200	P	±1000 V	0/3
TOTALS:					**0/9**

CDM ESD (ANSI/ESDA/JEDEC JS-002)
Classification Level: Class C1

CDM ESD

Lot ID	Product Name	Package	Step	Stress Voltage	Results
J93400XS	8070104xxxxxx	LGA1200	P	±250 V	0/3
J94200XS	8070104xxxxxx	LGA1200	P	±250 V	0/3
J94201XS	8070104xxxxxx	LGA1200	P	±250 V	0/3
TOTALS:					**0/9**

6.2 Direct Pin Zap Electrostatic Discharge

Stress Description:

Direct Pin Zap (DPZ) Electrostatic Discharge (ESD) testing is used to measure the device's sensitivity to various discharge events on a port with the device powered up in a system. These events can occur when a charged human touches a cable or peripheral device plugged into the port, when a charged cable is plugged into the port or when a charged notebook is discharged into a cable. Intel tests for DPZ issues with reference to Intel internal specification 25-0186 Direct Pin Zap Test Method. There is no industry specification available for this test.

Stress Conditions:

DPZ ESD testing is conducted in a manner similar to IEC specification 61000-4-2, except the discharges are applied directly to the conductors of the signal pins of the port under test. It is completed on the ports with shielded cables which have connections to the outside of the chassis. The stress is applied to the port of a representative system while it is powered up. Single ended and differential pair pins are all individually tested in a single mode configuration. Ten zaps are applied per pin at an interval of between 1 and 10 seconds.

Parts are tested on the representative system for functionality after zapping is complete. There are two different categories of potential failures: latch-up and lock-up. Latch-up is defined as either permanent damage to the device or a significant increase in current immediately after the zap. Lock-up is when a temporary loss of function occurs which requires user intervention to recover.

Stress Results:

DPZ ESD – Latch-up

Lot ID	Product Name	Package	Step	Stress Voltage	Results
J9400010Q	8070104xxxxxx	LGA1200	P	±1000 V	0/3
J9400011Q	8070104xxxxxx	LGA1200	P	±1000 V	0/3
J9410010Q	8070104xxxxxx	LGA1200	P	±1000 V	0/3
TOTALS:					**0/9**

DPZ ESD – Lock-up

Lot ID	Product Name	Package	Step	Stress Voltage	Results
J9400010Q	8070104xxxxxx	LGA1200	P	±600 V	0/3
J9400011Q	8070104xxxxxx	LGA1200	P	±600 V	0/3
J9410010Q	8070104xxxxxx	LGA1200	P	±600 V	0/3
TOTALS:					**0/9**

6.3 Latch-up

Stress Description:

Latch-up testing is performed on CMOS technologies to check the sensitivity of the product to parasitic bipolar action, often referred to as Silicon-Controlled Rectifier (SCR) latch-up. Two basic tests are completed to evaluate latch-up on a product: Vcc latch-up and I/O latch-up. Vcc Latch-up checks the product's sensitivity to Vcc over voltage while I/O latch-up checks the product's sensitivity to voltage over and undershoot on device pins.

Stress Conditions:

Latch-up is performed on a functional tester in accordance to JEDEC Standard JESD78. The stress is performed at hot temperature that meets the datasheet operating temperature. Icc measurements are taken before and after applying the stress, but without removing power. Post stress Icc measurements are compared to the pre-test results to check for latch-up conditions. Parts are functionally and parametrically tested after stress using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Vcc Latch-up

Lot ID	Product Name	Package	Step	Trigger Vcc	Hot (105°C)
J945001L	8070104xxxxxx	LGA1200	P	1.5x VCC max DC [B]	0/3
J947001L	8070104xxxxxx	LGA1200	P	1.5x VCC max DC [B]	0/3
J947002L	8070104xxxxxx	LGA1200	P	1.5x VCC max DC [B]	0/3
TOTALS:					**0/9**

I/O Latch-up

Lot ID	Product Name	Package	Step	Trigger Icc	Hot (105°C)
J952001L	8070104xxxxxx	LGA1200	P	±100 mA [A]	0/3
J952002L	8070104xxxxxx	LGA1200	P	±100 mA [A]	0/3
J002001L	8070104xxxxxx	LGA1200	P	±100 mA [A]	0/3
TOTALS:					**0/9**

A. Clamping voltage(s) for I/O Latch-up are VIH+0.5*(VIH-VIL) for positive trigger and VIL-0.5*(VIH-VIL) for negative trigger.
B. Trigger VCC at maximum AMR value.

6.4 Infant Mortality Evaluation (Early Life Failure Rate)

Stress Description:

An Infant Mortality Evaluation (IME) is performed to assess the latent defect portion of the operating reliability failure rate. The IME uses burn-in stressing, which is also used to monitor and control production material. Data from the IME is used to establish the required production burn-in time and control limits and to assess the individual product's latent defect Early-Life health on its process technology. IME results and fail mechanisms are statistically compared to model predictions to validate that the product is predictable to the technology baseline model.

Stress Conditions:

Units are stressed using dynamic patterns running in a controlled environmental chamber at an elevated Vcc and junction temperature. Actual stress Vcc and junction temperature for a given unit depends on the unit's power and position in the environmental chamber. The mean and variation are set to provide the necessary acceleration relative to the datasheet specifications. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Infant Mortality Evaluation

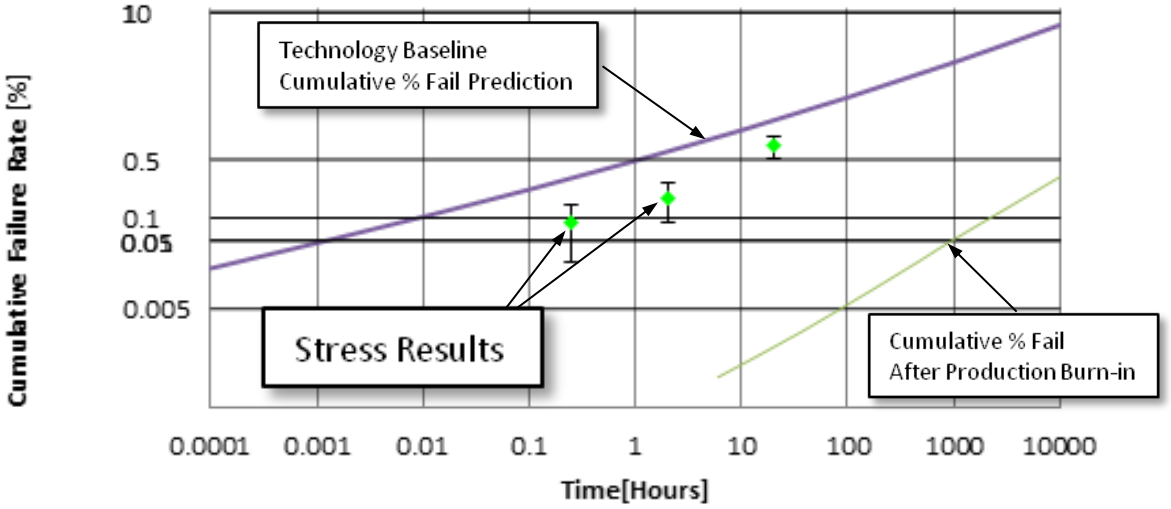
Lot ID	Product Name	Package	Step	Tj target	Vcc target	0.25 hrs	2 hrs	20 hrs
J944001X-J944021X, 21 lots	8070104xxxxxx	LGA1200	P	90°C	1.50 V	3/2111[1]	4/2108[2]	10/2104[3]
TOTALS:						**3/2111[1]**	**4/2108[2]**	**10/2104[3]**

Failure Summary:

1) 2 functional fails, 1 parametric fail
2) 2 functional fails, 2 parametric fails
3) 5 functional fails, 5 parametric fails

Infant Mortality Evaluation: Results Model Comparison

Cumulative % Fallout at Burn-in and "Use"



6.5 Temperature, Bias, and Operating Life (Extended Life Test)

Stress Description:

Extended Life Test (ELT) is used to assess the intrinsic electrical portion of the operating reliability failure rate.

Stress Conditions:

Extended Life Test (ELT) is used to assess the intrinsic electrical portion of the operating reliability failure rate. The ELT stress is distinct from Infant Mortality Evaluation (IME) described earlier in this section. Previously unstressed units are subjected to ELT stress conditions and the results are used to extract degradation parameters to ensure Intel reliability goals are met for the target market segment reference use conditions. Failures that would have been screened by our HVM flow are not included in the ELT results. ELT stress duration under accelerated conditions is defined to demonstrate the product lifetime across multiple mechanisms. Failures detected under the highly accelerated ELT stress conditions are analyzed and compared to models describing different failure mechanisms. For highly accelerated failure mechanisms, such as gate oxide time dependent dielectric breakdown (GOX TDDB), failures might be observed at intermediate ELT readouts if accelerated beyond use life. Reliability estimates covered in section 4 were calculated using empirically-derived models for the time-averaged use conditions described in this report. The reported ELT results showed predictability to those established models.

Stress Results:

Extended Life Test

Lot ID	Product Name	Package	Step	Tj target	Vcc target	1 hr	20 hrs	100 hrs
J940006E J940007E J940008E J940009E J940010E J940011E J941003E	8070104xxxxxx	LGA1200	P	90°C	1.5 V	1/249[1]	1/248[2]	1/247[3]
TOTALS:						**1/249[1]**	**1/248[2]**	**1/247[3]**

Failure Summary:

1) 1 parametric fail
2) 1 Functional fail
3) 1 parametric fail

6.6 Temperature Cycling

Stress Description:

Temperature Cycling (T/C) is performed to evaluate the mechanical integrity portion of the intrinsic operating reliability failure rate. Mechanical failure mechanisms such as solder joint fatigue, package cracking, and ILD (Interlayer Dielectric) cracking in the die and package are accelerated by this stress.

Stress Conditions:

This test is conducted in conformance with the procedures as defined in JEDEC Standard JESD22-A104. The devices are alternately exposed to -55°C to 125°C (Condition B) with a ramp rate of 15°C to 30°C per minute and a dwell time of 15 minutes. Heating and cooling are done by convection using temperature cycling chambers. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Temperature Cycling

Lot ID	Product Name	Package	Step	750 cycles
8942R907	8070104xxxxxx	LGA1200	P	0/96
8943Q036	8070104xxxxxx	LGA1200	P	0/80
8943Q106	8070104xxxxxx	LGA1200	P	0/131
TOTALS:				**0/307**

6.7 High Temperature Storage (Bake)

Stress Description:

A High Temperature Bake, with no applied electrical bias, is performed to evaluate the thermal integrity portion of the intrinsic operating reliability failure rate. The bake evaluation accelerates failure mechanisms such as single bit charge loss, bond degradation, ionic contamination, contact integrity, and metal void propagation.

Stress Conditions:

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A103 at an elevated temperature of 150°C (Condition B). Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

High Temperature Storage (Bake)

Lot ID	Product Name	Package	Step	504 hrs	1008 hrs
M829E109[A]	806840387xxxx	LGA1151	P	0/194	0/194
M829D841[A]	806840387xxxx	LGA1151	P	0/113	0/113
M829D838[A]	806840387xxxx	LGA1151	P	0/294	0/294
TOTALS:				**0/601**	**0/601**

A. This stress was performed on 806840387xxxx P-step processors, and the results are being shared with the 8070104xxxxxx Q-step processors quality and reliability verification. 806840387xxxx P-step processors envelope 8070104xxxxxx Q-step processors with regards to assembly materials, process & properties.

6.8 Accelerated Moisture Resistance – HAST

Stress Description:

Highly Accelerated Stress Test (HAST) is a high temperature/high humidity stress performed on non-hermetic devices to evaluate the moisture reliability portion of the intrinsic operating failure rate. Typical failure mechanisms from this stress include corrosion of metal and contamination induced threshold shifts due to moisture.

Stress Conditions:

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A118 (Unbiased). The devices are placed in an 110°C / 85%RH (Condition B) environment with no bias supplied. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Unbiased HAST

Lot ID	Product Name	Package	Step	100 hrs
8943S907	8070104xxxxxx	LGA1200	P	0/35
8941Q623	8070104xxxxxx	LGA1200	P	0/106
8943R907	8070104xxxxxx	LGA1200	P	0/167
TOTALS:				**0/308**

7.0 ADDITIONAL REFERENCES

Product Datasheet

Document Title: 10th Generation Intel® Processor Families Datasheet

This document is available post product launch at www.intel.com and can be found by performing a generic search on the web page using the products S-Spec. The document is found under Product Documentation and then under Technical Documents.

Thermal and Mechanical Design Guidelines

Document Title: Comet Lake S Platform Thermal and Mechanical Design Guide

This document is available post product launch at www.intel.com and can be found by performing a generic search on the web page using the S-Spec. The document is found under Product Documentation and then under Technical Documents.

Process certification document

Document Title: Intel® P1272 14nm Logic Technology Process Certification Report

The goal of this report is to provide customers with a reliability overview of Intel's CMOS logic processes used in fabrication. This will be relevant to the customer's Implementation of internal quality and reliability programs for products containing components manufactured using this technology.

This document is available upon request.

MAS Document

Document Title: Manufacturing with Intel® Desktop & Server Platforms - Shark Bay Mainstream Desktop & Denlow Server /Workstation Platforms

Intel(R) Manufacturing Advantage Service program (MAS) is designed to enable manufacturing customers and mitigate customer manufacturing risks. The MAS program shares Intel learning and BKMs, and deploys customer training materials in presentation, video, webinar and other formats. The MAS training materials are published through Intel Learning Network (http://learn.intel.com) and other websites. Please consult with your Intel field representatives or visit http://www.intel.com/design/quality/, Discover Customer Manufacturing Enabling and/or, refer to Resources to view and download the ESD/EOS prevention, rework BKMs, board flexure and component strain limit, shipping and handling, or other manufacturing videos or presentations topics.

8.0 REVISION HISTORY

Version	Date	Comments
Rev.0	April 2020	Initial Release

Appendix A

PRODUCT CHARACTERISTICS

General Information

Product Name	Intel ® Core™ Processor Intel® Xeon® Processor
Device Description	Intel ® Processor
S Spec	RH6R, RH6U, RH6Y, RH72, RH78, RH79, RH7H, RH8Y, RH8Z, RH91, RH93, RH94, RH95, RH96, RH97
Architecture	Comet Lake
Product Division	Client Computing Group
Die Size	22.2mm X 9.1mm
Transistor Count	3.95 Billion
Memory	20/16/12 MB Cache
I/O Count	Refer to Data Sheet
Vcc	Refer to Data Sheet
Icc	Refer to Data Sheet

PROCESS CHARACTERISTICS

General Information

Base Process Number	P1272
Process Name	14nm Logic
Fab Plant(s)[1]	Leixlip, Ireland; Kiryat Gat, Israel; Ocotillo, Arizona, United States; Hillsboro, Oregon, United States
Wafer Size	300 mm
Wafer Type	P –Epitaxially grown thin film on a P+ Si crystal substrate
Well Type	Dual well
Final Wafer/Die Thickness	500 um
Metal Layer Count	13 + 1 local contact routing

Gate Level Attributes

Gate Material	Dual work function metal stack
Gate Thickness	Not publicly disclosed
Thin Gate Oxide Thickness	Not publicly disclosed
Thick Gate Oxide Thickness	N/A
Minimum Gate Width	14 nm
Minimum Gate Pitch	Not publicly disclosed

Passivation Attributes

Passivation Material	Silicon nitride
Passivation Thickness	450 nm
Passivation Deposition	RECVD deposition technique
Die Overcoat Material	WPR (Wafer Passivation Resist)
Die Overcoat Method	Wafer Level

[1]Intel uses Copy Exactly methodologies to enable a Virtual Factory approach for Fab and Assembly/Test processes. Production sites may change during a product's manufacturing life, once appropriate certification and qualification have been accomplished to demonstrate output equivalence and compliance with applicable Quality & Reliability goals.

PACKAGE CHARACTERISTICS

General Information

Package Type	LGA1200
Assembly Plant(s)[1]	Chengdu, China; Ho Chi Minh City, Vietnam; Penang, Malaysia
Ball Land or Lead Count	1200
Package Dimensions	37.5 mm x 37.5 mm
Lead Finish Material	NiPdAu
Land or Solder Ball Pitch	0.91 µm
Flammability Classification[2]	Package and Underfill Compliant with (UL94-V0)

Additional Information

Moisture Level	MSL3
Shipping Media	JEDEC Compliant trays

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[2]Flammability classification determined using one or more standards: UL94, UL746C, or UL60950 or UL62368