



## Kabylake Intel(R) Firmware Support Package (FSP) Integration Guide

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# Chapter 1

## INTRODUCTION

### 1 Introduction

#### 1.1 Purpose

The purpose of this document is to describe the steps required to integrate the Intel® Firmware Support Package (FSP) into a boot loader solution. It supports Kabylake platforms with Kabylake/Skylake processor and Sunrise point Platform Controller Hub (PCH).

#### 1.2 Intended Audience

This document is targeted at all platform and system developers who need to consume FSP binaries in their boot loader solutions. This includes, but is not limited to: system BIOS developers, boot loader developers, system integrators, as well as end users.

#### 1.3 Related Documents

- *Platform Initialization (PI) Specification v1.4* located at <http://www.uefi.org/specifications>
- *UEFI Specification v2.5* located at <http://www.uefi.org/specifications>
- *Intel® Firmware Support Package: External Architecture Specification (EAS) v2.0* located at <http://www.intel.com/content/dam/www/public/us/en/documents/technical-specifications/fsp.pdf>
- *Boot Setting File Specification (BSF) v1.0* [https://firmware.intel.com/sites/default/files/BSF\\_1\\_0.pdf](https://firmware.intel.com/sites/default/files/BSF_1_0.pdf)
- *Binary Configuration Tool for Intel® Firmware Support Package* available at <http://www.intel.com/fsp>

#### 1.4 Acronyms and Terminology

Acronym	Definition
BCT	Binary Configuration Tool
BSF	Boot Setting File
BSP	Boot Strap Processor

BWG	BIOS Writer's Guide
CAR	Cache As Ram
CRB	Customer Reference Board
FIT	Firmware Interface Table
FSP	Firmware Support Package
FSP API	Firmware Support Package Interface
FW	Firmware
PCH	Platform Controller Hub
PMC	Power Management Controller
SBSP	System BSP
SMI	System Management Interrupt
SMM	System Management Mode
SPI	Serial Peripheral Interface
TSEG	Memory Reserved at the Top of Memory to be used as SMRAM
UPD	Updatable Product Data

## Chapter 2

# FSP OVERVIEW

### FSP Overview

#### 2.1 Technical Overview

The *Intel® Firmware Support Package (FSP)* provides chipset and processor initialization in a format that can easily be incorporated into many existing boot loaders.

The FSP will perform the necessary initialization steps as documented in the BWG including initialization of the CPU, memory controller, chipset and certain bus interfaces, if necessary.

FSP is not a stand-alone boot loader; therefore it needs to be integrated into a host boot loader to carry out other boot loader functions, such as: initializing non-Intel components, conducting bus enumeration, and discovering devices in the system and all industry standard initialization.

The FSP binary can be integrated easily into many different boot loaders, such as Coreboot, EDKII etc. and also into the embedded OS directly.

Below are some required steps for the integration:

- **Customizing** The static FSP configuration parameters are part of the FSP binary and can be customized by external tools that will be provided by Intel.
- **Rebasing** The FSP is not Position Independent Code (PIC) and the whole FSP has to be rebased if it is placed at a location which is different from the preferred address during build process.
- **Placing** Once the FSP binary is ready for integration, the boot loader build process needs to be modified to place this FSP binary at the specific rebasing location identified above.
- **Interfacing** The boot loader needs to add code to setup the operating environment for the FSP, call the FSP with correct parameters and parse the FSP output to retrieve the necessary information returned by the FSP.

#### 2.2 FSP Distribution Package

- The FSP distribution package contains the following:
  - FSP Binary
  - FSP Integration Guide
  - BSF Configuration File
  - Data Structure Header File
- The FSP configuration utility called BCT is available as a separate package. It can be downloaded from link mentioned in Section 1.3.

### 2.2.1 Package Layout

- **Docs (Auto generated)**
    - Kabylake\_FSP\_Integration\_Guide.pdf (this doc)
    - Kabylake\_FSP\_Integration\_Guide.chm
  - **Include**
    - [FspUpd.h](#), [FspmUpd.h](#) and [FspUpd.h](#) (FSP UPD structure and related definitions)
    - [GpioSampleDef.h](#) (Sample enum definitions for Gpio table)
  - KabylakeFspBinPkg.dec (EDKII declaration file for package)
  - Fsp.bsf (BSF file for configuring the data using BCT tool)
  - Fsp.fd (FSP Binary)
-

## Chapter 3

# FSP INTEGRATION

### 3 FSP Integration

#### 3.1 Assumptions Used in this Document

The FSP for the Kabylake platform is built with a preferred base address of 0xFF40000 and so the reference code provided in the document assumes that the FSP is placed at this base address during the final boot loader build. Users may rebase the FSP binary at a different location with Intel's Binary Configuration Tool (BCT) before integrating to the boot loader.

For other assumptions and conventions, please refer section 8 in the FSP External Architecture Specification version 2.0.

#### 3.2 Boot Flow

Please refer Chapter 7 in the FSP External Architecture Specification version 2.0 for Boot flow chart.

#### 3.3 FSP INFO Header

The FSP has an Information Header that provides critical information that is required by the bootloader to successfully interface with the FSP. The structure of the FSP Information Header is documented in the FSP External Architecture Specification version 2.0 with a HeaderRevision of 3.

#### 3.4 FSP Image ID and Revision

FSP information header contains an Image ID field and an Image Revision field that provide the identification and revision information of the FSP binary. It is important to verify these fields while integrating the FSP as AP<sub>↔</sub>I parameters could change over different FSP IDs and revisions. All the FSP FV segments(FSP-T, FSP-M and FSP-S) must have same FSP Image ID and revision number, using FV segments with different revision numbers in a single FSP image is not valid. The FSP API parameters documented in this integration guide are applicable for the Image ID and Revision specified as below.

The current FSP ImageId string in the FSP information header is **\$KBLFSP\$** and the ImageRevision field is **0x03070900.(3.7.9.0)**.

#### 3.5 FSP Global Data

FSP uses some amount of TempRam area to store FSP global data which contains some critical data like pointers to FSP information headers and UPD configuration regions, FSP/Bootloader stack pointers required for stack switching

etc. HPET Timer register(2) 0xFED00148 is reserved to store address of this global data, and hence boot loader should not use this register for any other purpose. If TempRAM initialization is done by boot loader, then HPET has to be initialized to the base so that access to this register will work fine.

### 3.6 FSP APIs

This release of the Kabylake FSP supports the all APIs required by the FSP External Architecture Specification version 2.0. The FSP information header contains the address offset for these APIs. Register usage is described in the FSP External Architecture Specification version 2.0. Any usage not described by the specification is described in the individual sections below.

The below sections will highlight any changes that are specific to this FSP release.

#### 3.6.1 TempRamInit API

Please refer Chapter 8.5 in the FSP External Architecture Specification version 2.0 for complete details including the prototype, parameters and return value details for this API.

TempRamInit does basic early initialization primarily setting up temporary RAM using cache. It returns ECX pointing to beginning of temporary memory and EDX pointing to end of temporary memory + 1. The total temporary ram currently available is from 0xFE0\_0000 to 0xFE4\_0000 out of which 0xFE0\_0000(ECX) to 0xFE3\_FF00(EDX) is usable area for both bootloader and FSP binary, remaining 0x100 bytes of space reserved by FSP for TempRamInit if temporary RAM initialization is done by FSP.

TempRamInit\*\* also sets up the code caching of the region passed CodeCacheBase and CodeCacheLength, which are input parameters to TempRamInitApi. If 0 is passed in for CodeCacheBase, the base used will be 4 GB - 1 - length to be code cached instead of starting from CodeCacheBase.

#### Note

: when programming MTRR CodeCacheLength will be reduced, if SKU LLC size is smaller than the requested.

It is a requirement for Firmware to have Firmware Interface Table (FIT), which contains pointers to each microcode update. The microcode update is loaded for all logical processors before reset vector. If more than microcode update for the CPU is present, the microcode update with the latest revision is loaded.

FSPT\_UPD.MicrocodeRegionBase\*\* and **FSPT\_UPD.MicrocodeRegionLength** are input parameters to TempRamInit API. If these values are 0, FSP will not attempt to update microcode. If a region is passed, then if a newer microcode update revision is in the region, it will be loaded by the FSP.

MTRRs are programmed to the default values to have the following memory map:

Memory range	Cache Attribute
0xFE000000 - 0x00040000	Write back
CodeCacheBase - CodeCacheLength	Write protect

#### 3.6.2 FspMemoryInit API

Please refer to Chapter 8.6 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

The **FspmUpdPtr** is pointer to **FSPM\_UPD** structure which is described in header file [FspmUpd.h](#).

Boot Loader must pass valid CAR region for FSP stack use through **FSPM\_UPD.FspmArchUpd.StackBase** and **FSPM\_UPD.FspmArchUpd.StackSize** UPDs.

The minimum FSP stack size required for this revision of FSP is 160KB, stack base is 0xFE17F00 by default.

The base address of HECI device (Bus 0, Device 22, Function 0) is required to be initialized prior to perform FspMemoryInit flow. The default address is programmed to 0xFED1A000.

Calculate memory map determining memory regions TSEG, IED, GTT, BDSM, ME stolen, Uncore PMRR, IOT, MOT, DPR, REMAP, TOLUD, TOUUD. Programming will be done at a different time.

### 3.6.3 TempRamExit API

Please refer to Chapter 8.7 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

If Boot Loader initializes the Temporary RAM (CAR) and skip calling **TempRamInit API**, it is expected that boot-loader must skip calling this API and bootloader will tear down the temporary memory area setup in the cache and bring the cache to normal mode of operation.

This revision of FSP doesn't have any fields/structure to pass as parameter for this API. Pass Null for *TempRamExitParamPtr*.

At the end of *TempRamExit* the original code and data caching are disabled. FSP will reconfigure all MTRRs as described in the table below for performance optimization.

Memory range	Cache Attribute
0x00000000 - 0x0009FFFF	Write back
0x000C0000 - Top of Low Memory	Write back
0xFF800000 - 0xFFFFFFFF (Flash region)	Write protect
0x1000000000 - Top of High Memory	Write back

If the boot loader wish to reconfigure the MTRRs differently, it can be overridden immediately after this API call.

### 3.6.4 FspSiliconInit API

Please refer to Chapter 8.8 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

The *FspUpdPtr* is pointer to **FSPS\_UPD** structure which is described in header file [FspUpd.h](#).

It is expected that boot loader will program MTRRs for SBSP as needed after **TempRamExit** but before entering **FspSiliconInit**. If MTRRs are not programmed properly, the boot performance might be impacted.

The region of 0x5\_8000 - 0x5\_8FFF is used by FspSiliconInit for starting APs. If this data is important to bootloader, then bootloader needs to preserve it before calling FspSiliconInit.

It is a requirement for bootloader to have Firmware Interface Table (FIT), which contains pointers to each microcode. The microcode is loaded for all cores before reset vector. If more than one microcode update for the CPU is present, the latest revision is loaded.

MicrocodeRegionBase and MicrocodeRegionLength are both input parameters to TempRamInit and UPD for SiliconInit API. UPD has priority and will be searched for a later revision than TempRamInit. If MicrocodeRegionBase and MicrocodeRegionLength values are 0, FSP will not attempt to update the microcode. If a microcode region is passed, and if a later revision of microcode is present in this region, FSP will load it.

FSP initializes PCH audio including selecting HD Audio verb table and initializes Codec.

PCH required initialization is done for the following HECI, USB, HSIO, Integrated Sensor Hub, Display, Sky Cam, Camera, PCI Express, Vt-d, straps (cores, hyper-threading, BIST, ...)

FSP initializes CPU features: XD, VMX, AES, IED, HDC, x(2)Apic, Intel® Processor Trace, Three strike counter, Machine check, Cache pre-fetchers, Core PMRR, Power management.

Initializes HECI, DMI, Internal Graphics. Publish EFI\_PEI\_GRAPHICS\_INFO\_HOB during normal boot but this HOB will not be published during S3 resume as FSP will not launch the PEI Graphics PEIM during S3 resume.

Programs SA Bars: MchBar, DmiBar, EpBar, GdxcBar, EDRAM (if supported). Please refer to section 2.8 (MemoryMap) for the corresponding Bar values. GttMmadr (0xDF000000) and GmAdr(0xC0000000) are temporarily programmed and cleared after use in FSP.

On normal boot CPU S3 Resume Data HOB is produced in this phase. This CPU S3 Resume Data HOB is described in section 4.4. Unless UPD SkipMplnit is enabled, on S3 resume, this data (not the entire HOB) must be passed through UPD CpuS3ResumeData, and optionally final S3 boot MTRRs is passed through UPD CpuS3ResumeMtrrData. During S3 resume unless SkipMplnit is enabled, GDT base and length and IDT base and length on APs are programmed to that of the BSP.

### 3.6.5 NotifyPhase API

Please refer Chapter 8.9 in the FSP External Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

#### 3.6.5.1 PostPciEnumeration Notification

This phase *EnumInitPhaseAfterPciEnumeration* is to be called after PCI enumeration but before execution of third party code such as option ROMs. Currently, nothing is done in this phase, but in the future updates, programming may be done in this phase.

#### 3.6.5.2 ReadyToBoot Notification

This phase *EnumInitPhaseReadyToBoot* is to be called before giving control to boot. It includes some final initialization steps recommended by the BWG, including power management settings, Send ME Message EOP (End of Post).

#### 3.6.5.3 EndOfFirmware Notification

This phase *EnumInitEndOfFirmware* is to be called before the firmware/preboot environment transfers management of all system resources to the OS or next level execution environment. It includes final locking of chipset registers

## 3.7 Memory Map

Below diagram represents the memory map allocated by FSP including the FSP specific regions.

## 3.8 Porting recommendation

Here listed some notes or recommendation when porting with FSP.

### 3.8.1 Locking PAM register

FSP 2.0 introduced EndOfFirmware Notify phase callback which is a recommended place for locking PAM registers so FSP by default implemented this way. If it is still too early to lock PAM registers then the PAM locking code inside FSP can be disabled by UPD -> [FSP\\_S\\_TEST\\_CONFIG](#) -> SkipPamLock or SA policy -> [\\_SI\\_PREMEM\\_POLICY\\_STRUCT](#) -> [SA\\_MISC\\_PEL\\_CONFIG](#) -> SkipPamLock, and platform or wrapper code should do the PAM locking right before booting OS (so do it outside FSP instead) by programming one PCI config space register as below.

This PAM locking step has to been applied in all boot paths including S3 resume. To lock PAM register:

```
MmioOr32 (B0: D0: F0: Register 0x80, BIT0)
```

### 3.8.2 Locking SMRAM register

Since SMRAM locking is recommended to be locked before any 3rd party OpROM execution and highly depending on platform code implementation, the FSP code by default will not lock it. The platform or FSP Wrapper code should lock SMRAM by below programming step before any 3rd party OpRom execution (and should be locked in S3 resume right before OS waking vector).

```
PciOr8 (B0: D0: F0: Register 0x88, BIT4); Note: it must be programmed by CF8/CFC Standard PCI access mechanism. (MMIO access will not work)
```

### 3.8.3 Locking SMI register

Global SMI bit is recommended to be locked before any 3rd party OpROM execution and highly depending on platform code implementation after SMM configuration. FSP by default will not lock it. Boot loader is responsible for



locking below registers after SMM configuration. Set AcpiBase + 0x30[0] to 1b to enable global SMI. Set PMC PCI offset A0h[4] = 1b to lock SMI.

### 3.8.4 Verify below settings are correct for your platforms

Settings	Values
PCIEXBAR_BASE_ADDRESS	0xE0000000 -> PciExBar
MCH_BASE_ADDRESS	0xFED10000 -> MchBar
DMI_BASE_ADDRESS	0xFED18000 -> DmiBar
EP_BASE_ADDRESS	0xFED19000 -> EpBar
EDRAM_BASE_ADDRESS	0xFED80000 -> EdramBar
DEFAULT_OPTION_ROM_TEMP_BAR	0x80000000 -> OpRomScanTempMmioBar
DEFAULT_OPTION_ROM_TEMP_MEM_LIMIT	0xC0000000 -> OpRomScanTempMmioLimit

#### Note

:

- It is recommended that you do not change these settings as it may require significant changes to the System Agent reference code.
- Those memory regions should be reserved from any memory service functions in platform code so it will not cause any conflict when other modules or drivers allocating memory resource.
- Boot Loader can use different value for PCIEXBAR\_BASE\_ADDRESS either by modifying the UPD (under FSP-T) or by overriding the PCIEXBAR (B0:D0:F0:R60h) before calling FspMemoryInit Api.
- Boot Loader should avoid using conflicting address when reprogramming PCIEXBAR\_BASE\_ADDRESS than the recommended one.

### 3.8.5 FSP\_STATUS\_RESET\_REQUIRED

As per FSP External Architecture Specification version 2.0, Any reset required in the FSP flow will be reported as return status FSP\_STATUS\_RESET\_REQUIREDx by the API. It is the bootloader responsibility to reset the system according to the reset type requested.

Below table specifies the return status returned by FSP API and the requested reset type.

FSP_STATUS_RESET_REQUIRED Code	Reset Type requested
0x40000001	Cold Reset
0x40000002	Warm Reset
0x40000003	Global Reset - Puts the system to Global reset through Heci or Full Reset through PCH
0x40000004	Reserved
0x40000005	Reserved
0x40000006	Reserved
0x40000007	Reserved
0x40000008	Reserved



## Chapter 4

# FSP OUTPUT

### 4 FSP Output

The FSP builds a series of data structures called the Hand-Off-Blocks (HOBs) as it progresses through initializing the silicon.

Please refer to the Platform Initialization (PI) Specification - Volume 3: Shared Architectural Elements specification for PI Architectural HOBs. Please refer Chapter 9 in the FSP External Architecture Specification version 2.0 for details about FSP Architectural HOBs.

Below section describe the HOBs not covered in the above two specifications.

#### 4.1 SMRAM Resource Descriptor HOB

The FSP will report the system SMRAM T-SEG range through a generic resource HOB if T-SEG is enabled. The owner field of the HOB identifies the owner as T-SEG.

```
#define FSP_HOB_RESOURCE_OWNER_TSEG_GUID \
{ 0xd038747c, 0xd00c, 0x4980, { 0xb3, 0x19, 0x49, 0x01, 0x99, 0xa4, 0x7d, 0x55 } }
```

#### 4.2 SMBIOS INFO HOB

The FSP will report the SMBIOS through a HOB with below GUID. This information can be consumed by the bootloader to produce the SMBIOS tables. These structures are included as part of [MemInfoHob.h](#) , [SmbiosCacheInfoHob.h](#) & [SmbiosProcessorInfoHob.h](#). Note: The Smbios Cache Info Hob & Smbios Processor Info Hob won't be published on S3 boot.

```
#define SI_MEMORY_INFO_DATA_HOB_GUID \
{ 0x9b2071d4, 0xb054, 0x4e0c, { 0x8d, 0x09, 0x11, 0xcf, 0x8b, 0x9f, 0x03, 0x23 } };

typedef struct {
    MrcDimmStatus Status;           ///< See MrcDimmStatus for the definition of this field.
    UINT8 DimmId;
    UINT32 DimmCapacity;           ///< DIMM size in MBytes.
    UINT16 MfgId;
    UINT8 ModulePartNum[20];       ///< Module part number for DDR3 is 18 bytes however for DDR4
    20 bytes as per JEDEC Spec, so reserving 20 bytes
    UINT8 RankInDimm;             ///< The number of ranks in this DIMM.
    UINT8 SpdDramDeviceType;       ///< Save SPD DramDeviceType information needed for SMBIOS
    structure creation.
    UINT8 SpdModuleType;          ///< Save SPD ModuleType information needed for SMBIOS
    structure creation.
    UINT8 SpdModuleMemoryBusWidth; ///< Save SPD ModuleMemoryBusWidth information needed for
    SMBIOS structure creation.
    UINT8 SpdSave[MAX_SPD_SAVE_DATA]; ///< Save SPD Manufacturing information needed for SMBIOS
    structure creation.
} DIMM_INFO;

typedef struct {
```

```

    UINT8      Status;                ///< Indicates whether this channel should be used.
    UINT8      ChannelId;
    UINT8      DimmCount;             ///< Number of valid DIMMs that exist in the channel.
    MRC_CH_TIMING Timing[MAX_PROFILE]; ///< The channel timing values.
    DIMM_INFO   Dimm[MAX_DIMM];       ///< Save the DIMM output characteristics.
} CHANNEL_INFO;

typedef struct {
    UINT8      Status;                ///< Indicates whether this controller should be used.
    UINT16     DeviceId;              ///< The PCI device id of this memory controller.
    UINT8      RevisionId;            ///< The PCI revision id of this memory controller.
    UINT8      ChannelCount;          ///< Number of valid channels that exist on the controller.
    CHANNEL_INFO Channel[MAX_CH];     ///< The following are channel level definitions.
} CONTROLLER_INFO;

typedef struct {
    EFI_HOB_GUID_TYPE EfiHobGuidType;
    UINT8      Revision;
    UINT16     DataWidth;
    ///< As defined in SMBIOS 3.0 spec
    ///< Section 7.18.2 and Table 75
    UINT8      DdrType;               ///< DDR type: DDR3, DDR4, or LPDDR3
    UINT32     Frequency;             ///< The system's common memory controller frequency in MT/s.
    ///< As defined in SMBIOS 3.0 spec
    ///< Section 7.17.3 and Table 72
    UINT8      ErrorCorrectionType;

    SiMrcVersion Version;
    UINT32     FreqMax;
    BOOLEAN    EccSupport;
    UINT8      MemoryProfile;
    UINT32     TotalPhysicalMemorySize;
    BOOLEAN    XmpProfileEnable;
    UINT8      Ratio;
    UINT8      RefClk;
    UINT32     VddVoltage[MAX_PROFILE];
    CONTROLLER_INFO Controller[MAX_NODE];
} MEMORY_INFO_DATA_HOB;

#define SI_MEMORY_PLATFORM_DATA_HOB \
    { 0x6210d62f, 0x418d, 0x4999, { 0xa2, 0x45, 0x22, 0x10, 0x0a, 0x5d, 0xea, 0x44 } }

typedef struct {
    UINT8      Revision;
    UINT8      Reserved[3];
    UINT32     BootMode;
    UINT32     TsegSize;
    UINT32     TsegBase;
    UINT32     PrmrrSize;
    UINT32     PrmrrBase;
    UINT32     GttBase;
    UINT32     MmioSize;
    UINT32     PciEBaseAddress;
} MEMORY_PLATFORM_DATA;

typedef struct {
    EFI_HOB_GUID_TYPE EfiHobGuidType;
    MEMORY_PLATFORM_DATA Data;
    UINT8      *Buffer;
} MEMORY_PLATFORM_DATA_HOB;

#define SMBIOS_CACHE_INFO_HOB_GUID \
    { 0xd805b74e, 0x1460, 0x4755, {0xbb, 0x36, 0x1e, 0x8c, 0x8a, 0xd6, 0x78, 0xd7} }

///<
///< SMBIOS Cache Info HOB Structure
///<
typedef struct {
    UINT16     ProcessorSocketNumber;
    UINT16     NumberOfCacheLevels;   ///< Based on Number of Cache Types L1/L2/L3
    UINT8      SocketDesignationStrIndex; ///< String Index in the string Buffer. Example "L1-CACHE"
    UINT16     CacheConfiguration;    ///< Format defined in SMBIOS Spec v3.0 Section 7.8 Table 36
    UINT16     MaxCacheSize;           ///< Format defined in SMBIOS Spec v3.0 Section 7.8.1
    UINT16     InstalledSize;          ///< Format defined in SMBIOS Spec v3.0 Section 7.8.1
    UINT16     SupportedSramType;       ///< Format defined in SMBIOS Spec v3.0 Section 7.8.2
    UINT16     CurrentSramType;         ///< Format defined in SMBIOS Spec v3.0 Section 7.8.2
    UINT8      CacheSpeed;             ///< Cache Speed in nanoseconds. 0 if speed is unknown.
    UINT8      ErrorCorrectionType;     ///< ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.3
    UINT8      SystemCacheType;        ///< ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.4
    UINT8      Associativity;          ///< ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.5
    ///

```

---

```

/// SMBIOS Processor Info HOB Structure
///
typedef struct {
    UINT16    TotalNumberOfSockets;
    UINT16    CurrentSocketNumber;
    UINT8     ProcessorType;          ///< ENUM defined in SMBIOS Spec v3.0 Section 7.5.1
    ///This info is used for both ProcessorFamily and ProcessorFamily2 fields
    ///See ENUM defined in SMBIOS Spec v3.0 Section 7.5.2
    UINT16    ProcessorFamily;
    UINT8     ProcessorManufacturerStrIndex; ///< Index of the String in the String Buffer
    UINT64    ProcessorId;                ///< ENUM defined in SMBIOS Spec v3.0 Section 7.5.3
    UINT8     ProcessorVersionStrIndex;    ///< Index of the String in the String Buffer
    UINT8     Voltage;                    ///< Format defined in SMBIOS Spec v3.0 Section 7.5.4
    UINT16    ExternalClockInMHz;         ///< External Clock Frequency. Set to 0 if unknown.
    UINT16    CurrentSpeedInMHz;          ///< Snapshot of current processor speed during boot
    UINT8     Status;                     ///< Format defined in the SMBIOS Spec v3.0 Table 21
    UINT8     ProcessorUpgrade;           ///< ENUM defined in SMBIOS Spec v3.0 Section 7.5.5
    ///This info is used for both CoreCount & CoreCount2 fields
    /// See detailed description in SMBIOS Spec v3.0 Section 7.5.6
    UINT16    CoreCount;
    ///This info is used for both CoreEnabled & CoreEnabled2 fields
    ///See detailed description in SMBIOS Spec v3.0 Section 7.5.7
    UINT16    EnabledCoreCount;
    ///This info is used for both ThreadCount & ThreadCount2 fields
    /// See detailed description in SMBIOS Spec v3.0 Section 7.5.8
    UINT16    ThreadCount;
    UINT16    ProcessorCharacteristics;    ///< Format defined in SMBIOS Spec v3.0 Section 7.5.9
    /// String Buffer - each string terminated by NULL "0x00"
    /// String buffer terminated by double NULL "0x0000"
} SMBIOS_PROCESSOR_INFO;

```

### 4.3 CHIPSETINIT INFO HOB

The FSP will report the ChipsetInit CRC through a HOB with below GUID. This information can be consumed by the bootloader to check if ChipsetInit CRC is matched between BIOS and ME. These structures are included as part of [FspUpd.h](#)

```

#define CHIPSETINIT_INFO_HOB_GUID \
{ 0xc1392859, 0x1f65, 0x446e, { 0xb3, 0xf5, 0x84, 0x35, 0xfc, 0xc7, 0xd1, 0xc4 } }

///
/// The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC.
///
typedef struct {
    UINT8     Revision;
    UINT8     Rsvd[3];
    UINT16    MeChipInitCrc;
    UINT16    BiosChipInitCrc;
} CHIPSET_INIT_INFO;

```

### 4.4 CPU S3 Resume Data HOB

The FSP will report the CPU S3 Resume Data through a GUIDED HOB with below GUID. This data (not the entire HOB) must be passed during S3 resume passed in UPD CpuS3ResumeData except if UPD SkipMplInit is enabled.

```

#define CPU_S3_RESUME_DATA_HOB_GUID \
{ 0x3972d4c1, 0xf206, 0x463f, { 0x80, 0xa4, 0xd9, 0x62, 0x79, 0x0a, 0xe5, 0x49 } }

```

---



## Chapter 5

# FSP POSTCODE

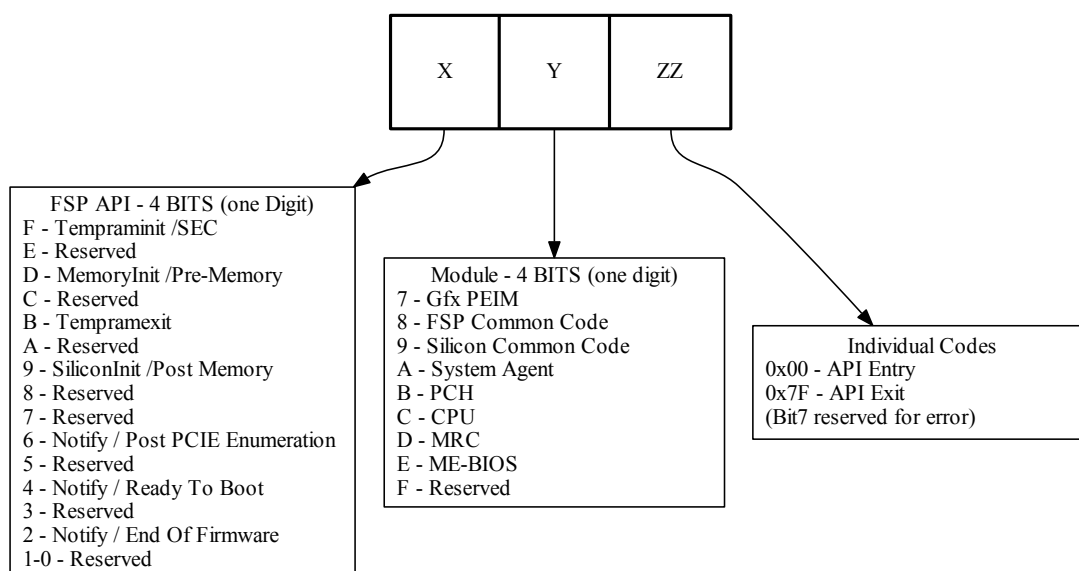
### 5 FSP PostCode

The FSP outputs 16 bit postcode to indicate which API and in which module the execution is happening.

Bit Range	Description
Bit15 - Bit12 (X)	used to indicate the phase/api under which the code is executing
Bit11 - Bit8 (Y)	used to indicate the module
Bit7 (ZZ bit 7)	reserved for error
Bit6 - Bit0 (ZZ)	individual codes

#### 5.1 PostCode Info

Below diagram represents the 16 bit PostCode usage in FSP.



#### 5.1.1 TempRamInit API Status Codes (0xFxxx)

PostCode	Module	Description
0x0000	FSP	TempRamInit API Entry (The change in upper byte is due to not enabling of the Port81 early in the boot)
0x007F	FSP	TempRamInit API Exit

### 5.1.2 FspMemoryInit API Status Codes (0xDxxx)

PostCode	Module	Description
0xD800	FSP	FspMemoryInit API Entry
0xD87F	FSP	FSpMemoryInit API Exit
0xDA00	SA	Pre-Mem Salnit Entry
0xDA01	SA	DeviceConfigurePreMem Start
0xDA02	SA	OverrideDev0Did Start
0xDA04	SA	OverrideDev2Did Start
0xDA06	SA	Programming SA Bars
0xDA08	SA	Install SA HOBs
0xDA0A	SA	Reporting SA PCIe code version
0xDA0C	SA	SaSvlnit Start
0xDA10	SA	Initializing DMI
0xDA1F	SA	Initializing DMI/OPI Max PayLoad Size
0xDA20	SA	Initializing SwitchableGraphics
0xDA30	SA	Initializing SA PCIe
0xDA3F	SA	Programming PEG credit values Start
0xDA40	SA	Initializing DMI Tc/Vc mapping
0xDA42	SA	CheckOffboardPcieVga
0xDA44	SA	CheckAndInitializePegVga
0xDA50	SA	Initializing Graphics
0xDA7F	SA	Pre-Mem Salnit Exit
0xDB00	PCH	PCH API Entry
0xDC00	CPU	Pre-Mem Entry
0xDC7F	CPU	Pre-Mem Exit

### 5.1.3 TempRamExit API Status Codes (0xBxxx)

PostCode	Module	Description
0xB800	FSP	TempRamExit API Entry
0xB87F	FSP	TempRamExit API Exit

### 5.1.3 FspSiliconInit API Status Codes (0x9xxx)

PostCode	Module	Description
0x9800	FSP	FspSiliconInit API Entry
0x987F	FSP	FspSiliconInit API Exit
0x9A00	SA	Post-Mem Salnit Entry
0x9A01	SA	DeviceConfigure Start
0x9A02	SA	UpdateSaHobPostMem Start
0x9A03	SA	Initializing Pei Display
0x9A04	SA	PeiGraphicsNotifyCallback Entry



0x9A05	SA	CallPpiAndFillFrameBuffer
0x9A06	SA	GraphicsPpiInit
0x9A07	SA	GraphicsPpiGetMode
0x9A08	SA	FillFrameBufferAndShowLogo
0x9A0F	SA	PeiGraphicsNotifyCallback Exit
0x9A10	SA	Initializing SA Overclocking
0x9A14	SA	Initializing SA SkyCam device
0x9A16	SA	Initializing SA GMM device
0x9A18	SA	Internal Device and Misc Configurations
0x9A1A	SA	SaProgramLlcWays Start
0x9A20	SA	Initializing PciExpressInitPostMem
0x9A30	SA	Initializing Vtd
0x9A32	SA	Initializing Pvp
0x9A34	SA	PeiInstallSmmAccessPpi Start
0x9A36	SA	EdramWa Start
0x9A4F	SA	Post-Mem Salnit Exit
0x9A50	SA	SaSecurityLock Start
0x9A5F	SA	SaSecurityLock End
0x9A60	SA	SaSResetComplete Entry
0x9A61	SA	Set BIOS_RESET_CPL to indicate all configurations complete
0x9A62	SA	SaSvlnit2 Start
0x9A63	SA	GraphicsPmInit Start
0x9A64	SA	SaPeiPolicyDump Start
0x9A6F	SA	SaSResetComplete Exit
0x9A70	SA	SaS3ResumeAtEndOfPei Callback Entry
0x9A7F	SA	SaS3ResumeAtEndOfPei Callback Exit
0x9B7F	PCH	Post-Mem ScInit Entry
0x9B01	PCH	Post-Mem Program HSIO ModPHY settings
0x9B02	PCH	Post-Mem SMBus configuration
0x9B03	PCH	Post-Mem LPC configuration
0x9B04	PCH	Post-Mem SATA initialization
0x9B05	PCH	Post-Mem PCIe initialization
0x9B06	PCH	Post-Mem xHCI initialization
0x9B07	PCH	Post-Mem xDCI initialization
0x9B08	PCH	Post-Mem HD Audio initialization
0x9B09	PCH	Post-Mem GMM configuration
0x9B0A	PCH	Post-Mem LPSS initialization
0x9B0B	PCH	Post-Mem SCS initialization
0x9B0C	PCH	Post-Mem ISH initialization
0x9B0D	PCH	Post-Mem ITSS configuration
0x9B40	PCH	Post-Mem OnEndOfPEI Entry
0x9B4F	PCH	Post-Mem OnEndOfPEI Exit
0x9B7F	PCH	Post-Mem ScInit Exit

0x9C00	CPU	Post-Mem Entry
0x9C7F	CPU	Post-Mem Exit

#### 5.1.4 NotifyPhase API Status Codes (0x6xxx)

PostCode	Module	Description
0x6800	FSP	NotifyPhase API Entry
0x687F	FSP	NotifyPhase API Exit

---

## Chapter 6

# Class Index

### 6.1 Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

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## Chapter 7

# File Index

### 7.1 File List

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## Chapter 8

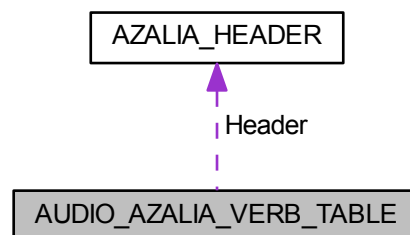
# Class Documentation

### 8.1 AUDIO\_AZALIA\_VERB\_TABLE Struct Reference

Audio Azalia Verb Table structure.

```
#include <FspsUpd.h>
```

Collaboration diagram for AUDIO\_AZALIA\_VERB\_TABLE:



#### Public Attributes

- [AZALIA\\_HEADER](#) Header  
*AZALIA PCH header.*
- `UINT32 *` [Data](#)  
*Pointer to the data buffer. Its length is specified in the header.*

#### 8.1.1 Detailed Description

Audio Azalia Verb Table structure.

Definition at line 58 of file FspsUpd.h.

The documentation for this struct was generated from the following file:

- [FspsUpd.h](#)

## 8.2 AZALIA\_HEADER Struct Reference

Azalia Header structure.

```
#include <FspsUpd.h>
```

### Public Attributes

- [UINT16 VendorId](#)  
*Codec Vendor ID.*
- [UINT16 DeviceId](#)  
*Codec Device ID.*
- [UINT8 RevisionId](#)  
*Revision ID of the codec. 0xFF matches any revision.*
- [UINT8 SdiNum](#)  
*SDI number, 0xFF matches any SDI.*
- [UINT16 DataDwords](#)  
*Number of data DWORDs pointed by the codec data buffer.*
- [UINT32 Reserved](#)  
*Reserved for future use. Must be set to 0.*

### 8.2.1 Detailed Description

Azalia Header structure.

Definition at line 46 of file FspsUpd.h.

The documentation for this struct was generated from the following file:

- [FspsUpd.h](#)

## 8.3 DIMM\_INFO Struct Reference

Memory SMBIOS & OC Memory Data Hob.

```
#include <MemInfoHob.h>
```

### Public Attributes

- [UINT8 Status](#)  
*See MrcDimmStatus for the definition of this field.*
  - [UINT32 DimmCapacity](#)  
*DIMM size in MBytes.*
  - [UINT8 ModulePartNum](#) [20]  
*Module part number for DDR3 is 18 bytes however for DRR4 20 bytes as per JEDEC Spec, so reserving 20 bytes.*
  - [UINT8 RankInDimm](#)  
*The number of ranks in this DIMM.*
  - [UINT8 SpdDramDeviceType](#)  
*Save SPD DramDeviceType information needed for SMBIOS structure creation.*
  - [UINT8 SpdModuleType](#)  
*Save SPD ModuleType information needed for SMBIOS structure creation.*
  - [UINT8 SpdModuleMemoryBusWidth](#)
-



*Save SPD ModuleMemoryBusWidth information needed for SMBIOS structure creation.*

- UINT8 [SpdSave](#) [[MAX\\_SPD\\_SAVE](#)]

*Save SPD Manufacturing information needed for SMBIOS structure creation.*

### 8.3.1 Detailed Description

Memory SMBIOS & OC Memory Data Hob.

Definition at line 188 of file MemInfoHob.h.

The documentation for this struct was generated from the following file:

- [MemInfoHob.h](#)

## 8.4 FSP\_M\_CONFIG Struct Reference

Fsp M Configuration.

```
#include <FspmUpd.h>
```

### Public Attributes

- UINT64 [PlatformMemorySize](#)  
*Offset 0x0040 - Platform Reserved Memory Size The minimum platform memory size required to pass control into DXE.*
- UINT32 [MemorySpdPtr00](#)  
*Offset 0x0048 - Memory SPD Pointer Channel 0 Dimm 0 Pointer to SPD data in Memory.*
- UINT32 [MemorySpdPtr01](#)  
*Offset 0x004C - Memory SPD Pointer Channel 0 Dimm 1 Pointer to SPD data in Memory.*
- UINT32 [MemorySpdPtr10](#)  
*Offset 0x0050 - Memory SPD Pointer Channel 1 Dimm 0 Pointer to SPD data in Memory.*
- UINT32 [MemorySpdPtr11](#)  
*Offset 0x0054 - Memory SPD Pointer Channel 1 Dimm 1 Pointer to SPD data in Memory.*
- UINT16 [MemorySpdDataLen](#)  
*Offset 0x0058 - SPD Data Length Length of SPD Data 0x100:256 Bytes, 0x200:512 Bytes.*
- UINT8 [DqByteMapCh0](#) [12]  
*Offset 0x005A - Dq Byte Map CH0 Dq byte mapping between CPU and DRAM, Channel 0: board-dependent.*
- UINT8 [DqByteMapCh1](#) [12]  
*Offset 0x0066 - Dq Byte Map CH1 Dq byte mapping between CPU and DRAM, Channel 1: board-dependent.*
- UINT8 [DqsMapCpu2DramCh0](#) [8]  
*Offset 0x0072 - Dqs Map CPU to DRAM CH 0 Set Dqs mapping relationship between CPU and DRAM, Channel 0: board-dependent.*
- UINT8 [DqsMapCpu2DramCh1](#) [8]  
*Offset 0x007A - Dqs Map CPU to DRAM CH 1 Set Dqs mapping relationship between CPU and DRAM, Channel 1: board-dependent.*
- UINT16 [RcompResistor](#) [3]  
*Offset 0x0082 - RcompResister settings Indicates RcompReister settings: Board-dependent.*
- UINT16 [RcompTarget](#) [5]  
*Offset 0x0088 - RcompTarget settings RcompTarget settings: board-dependent.*
- UINT8 [DqPinsInterleaved](#)  
*Offset 0x0092 - Dqs Pins Interleaved Setting Indicates DqPinsInterleaved setting: board-dependent \$EN\_DIS.*
- UINT8 [CaVrefConfig](#)

- Offset 0x0093 - VREF\_CA CA Vref routing: board-dependent 0:VREF\_CA goes to both CH\_A and CH\_B, 1: VREF\_CA to CH\_A and VREF\_DQ\_A to CH\_B, 2:VREF\_CA to CH\_A and VREF\_DQ\_B to CH\_B.
- UINT8 [SmramMask](#)  
Offset 0x0094 - Smram Mask The SMM Regions AB-SEG and/or H-SEG reserved 0: Neither, 1:AB-SEG, 2:H-SEG, 3: Both.
  - UINT8 [MrcFastBoot](#)  
Offset 0x0095 - MRC Fast Boot Enables/Disable the MRC fast path thru the MRC \$EN\_DIS.
  - UINT8 [UnusedUpdSpace0](#) [2]  
Offset 0x0096.
  - UINT32 [IedSize](#)  
Offset 0x0098 - Intel Enhanced Debug Intel Enhanced Debug (IED): 0=Disabled, 0x400000=Enabled and 4MB SDRAM occupied 0 : Disable, 0x400000 : Enable.
  - UINT32 [TsegSize](#)  
Offset 0x009C - Tseg Size Size of SMRAM memory reserved.
  - UINT16 [MmioSize](#)  
Offset 0x00A0 - MMIO Size Size of MMIO space reserved for devices.
  - UINT8 [ProbelessTrace](#)  
Offset 0x00A2 - Probeless Trace Probeless Trace: 0=Disabled, 1=Enable.
  - UINT8 [UnusedUpdSpace1](#) [2]  
Offset 0x00A3.
  - UINT8 [SmbusEnable](#)  
Offset 0x00A5 - Enable SMBus Enable/disable SMBus controller.
  - UINT8 [EnableTraceHub](#)  
Offset 0x00A6 - Enable Trace Hub Enable/disable Trace Hub function.
  - UINT8 [DpSscMarginEnable](#)  
Offset 0x00A7 - DpSscMarginEnable Enable/Disable.
  - UINT8 [UnusedUpdSpace2](#) [59]  
Offset 0x00A8.
  - UINT8 [IgdDvmt50PreAlloc](#)  
Offset 0x00E3 - Internal Graphics Pre-allocated Memory Size of memory preallocated for internal graphics.
  - UINT8 [InternalGfx](#)  
Offset 0x00E4 - Internal Graphics Enable/disable internal graphics.
  - UINT8 [ApertureSize](#)  
Offset 0x00E5 - Aperture Size Select the Aperture Size.
  - UINT8 [SaGv](#)  
Offset 0x00E6 - SA GV System Agent dynamic frequency support and when enabled memory will be training at two different frequencies.
  - UINT8 [RMT](#)  
Offset 0x00E7 - Rank Margin Tool Enable/disable Rank Margin Tool.
  - UINT16 [DdrFreqLimit](#)  
Offset 0x00E8 - DDR Frequency Limit Maximum Memory Frequency Selections in Mhz.
  - UINT8 [UserBd](#)  
Offset 0x00EA - Board Type MrcBoardType, Options are 0=Mobile/Mobile Halo, 1=Desktop/DT Halo, 5=ULT/ULX/Mobile Halo, 7=UP Server 0:Mobile/Mobile Halo, 1:Desktop/DT Halo, 5:ULT/ULX/Mobile Halo, 7:UP Server.
  - UINT8 [UnusedUpdSpace3](#) [105]  
Offset 0x00EB.
  - UINT32 [MmaTestContentPtr](#)  
Offset 0x0154 - MMA Test Content Pointer Pointer to MMA Test Content in Memory.
  - UINT32 [MmaTestContentSize](#)  
Offset 0x0158 - MMA Test Content Size Size of MMA Test Content in Memory.
  - UINT32 [MmaTestConfigPtr](#)  
Offset 0x015C - MMA Test Config Pointer Pointer to MMA Test Config in Memory.
-

- UINT32 [MmaTestConfigSize](#)  
*Offset 0x0160 - MMA Test Config Size Size of MMA Test Config in Memory.*
  - UINT8 [UnusedUpdSpace4](#) [19]  
*Offset 0x0164.*
  - UINT8 [SpdProfileSelected](#)  
*Offset 0x0177 - SPD Profile Selected Select DIMM timing profile.*
  - UINT16 [VddVoltage](#)  
*Offset 0x0178 - Memory Voltage Memory Voltage Override (Vddq).*
  - UINT8 [RefClk](#)  
*Offset 0x017A - Memory Reference Clock Automatic, 100MHz, 133MHz.*
  - UINT8 [Ratio](#)  
*Offset 0x017B - Memory Ratio Automatic or the frequency will equal ratio times reference clock.*
  - UINT8 [OddRatioMode](#)  
*Offset 0x017C - QCLK Odd Ratio Adds 133 or 100 MHz to QCLK frequency, depending on RefClk \$EN\_DIS.*
  - UINT8 [tCL](#)  
*Offset 0x017D - tCL CAS Latency, 0: AUTO, max: 31.*
  - UINT16 [tFAW](#)  
*Offset 0x017E - tFAW Min Four Activate Window Delay Time, 0: AUTO, max: 63.*
  - UINT16 [tRAS](#)  
*Offset 0x0180 - tRAS RAS Active Time, 0: AUTO, max: 64.*
  - UINT8 [tCWL](#)  
*Offset 0x0182 - tCWL Min CAS Write Latency Delay Time, 0: AUTO, max: 20.*
  - UINT8 [tRCDtRP](#)  
*Offset 0x0183 - tRCD/tRP RAS to CAS delay time and Row Precharge delay time, 0: AUTO, max: 63.*
  - UINT16 [tREFI](#)  
*Offset 0x0184 - tREFI Refresh Interval, 0: AUTO, max: 65535.*
  - UINT16 [tRFC](#)  
*Offset 0x0186 - tRFC Min Refresh Recovery Delay Time, 0: AUTO, max: 1023.*
  - UINT8 [tRRD](#)  
*Offset 0x0188 - tRRD Min Row Active to Row Active Delay Time, 0: AUTO, max: 15.*
  - UINT8 [tRTP](#)  
*Offset 0x0189 - tRTP Min Internal Read to Precharge Command Delay Time, 0: AUTO, max: 15.*
  - UINT8 [tWR](#)  
*Offset 0x018A - tWR Min Write Recovery Time, 0: AUTO, legal values: 5, 6, 7, 8, 10, 12, 14, 16, 18, 20, 24 0:Auto, 5:5, 6:6, 7:7, 8:8, 10:10, 12:12, 14:14, 16:16, 18:18, 20:20, 24:24.*
  - UINT8 [tWTR](#)  
*Offset 0x018B - tWTR Min Internal Write to Read Command Delay Time, 0: AUTO, max: 28.*
  - UINT8 [NModeSupport](#)  
*Offset 0x018C - NMode System command rate, range 0-2, 0 means auto, 1 = 1N, 2 = 2N.*
  - UINT8 [DlIBwEn0](#)  
*Offset 0x018D - DlIBwEn[0] DlIBwEn[0], for 1067 (0..7)*
  - UINT8 [DlIBwEn1](#)  
*Offset 0x018E - DlIBwEn[1] DlIBwEn[1], for 1333 (0..7)*
  - UINT8 [DlIBwEn2](#)  
*Offset 0x018F - DlIBwEn[2] DlIBwEn[2], for 1600 (0..7)*
  - UINT8 [DlIBwEn3](#)  
*Offset 0x0190 - DlIBwEn[3] DlIBwEn[3], for 1867 and up (0..7)*
  - UINT8 [CmdTriStateDis](#)  
*Offset 0x0191 - Command Tristate Support Enable/Disable Command Tristate; 0: **Enable**; 1: Disable.*
  - UINT8 [UnusedUpdSpace5](#) [14]  
*Offset 0x0192.*
-

- UINT32 [Heci1BarAddress](#)  
*Offset 0x01A0 - HECI1 BAR address BAR address of HECI1.*
  - UINT32 [Heci2BarAddress](#)  
*Offset 0x01A4 - HECI2 BAR address BAR address of HECI2.*
  - UINT32 [Heci3BarAddress](#)  
*Offset 0x01A8 - HECI3 BAR address BAR address of HECI3.*
  - UINT8 [HeciTimeouts](#)  
*Offset 0x01AC - HECI Timeouts Enable/Disable.*
  - UINT8 [UnusedUpdSpace6](#) [115]  
*Offset 0x01AD.*
  - UINT16 [SgDelayAfterPwrEn](#)  
*Offset 0x0220 - SG dGPU Power Delay SG dGPU delay interval after power enabling: 0=Minimal, 1000=Maximum, default is 300=300 microseconds.*
  - UINT16 [SgDelayAfterHoldReset](#)  
*Offset 0x0222 - SG dGPU Reset Delay SG dGPU delay interval for Reset complete: 0=Minimal, 1000=Maximum, default is 100=100 microseconds.*
  - UINT16 [MmioSizeAdjustment](#)  
*Offset 0x0224 - MMIO size adjustment for AUTO mode Positive number means increasing MMIO size, Negative value means decreasing MMIO size: 0 (Default)=no change to AUTO mode MMIO size.*
  - UINT8 [DmiGen3ProgramStaticEq](#)  
*Offset 0x0226 - Enable/Disable DMI GEN3 Static EQ Phase1 programming Program DMI Gen3 EQ Phase1 Static Presets.*
  - UINT8 [Peg0Enable](#)  
*Offset 0x0227 - Enable/Disable PEG 0 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.*
  - UINT8 [Peg1Enable](#)  
*Offset 0x0228 - Enable/Disable PEG 1 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.*
  - UINT8 [Peg2Enable](#)  
*Offset 0x0229 - Enable/Disable PEG 2 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.*
  - UINT8 [Peg0MaxLinkSpeed](#)  
*Offset 0x022A - PEG 0 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.*
  - UINT8 [Peg1MaxLinkSpeed](#)  
*Offset 0x022B - PEG 1 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.*
  - UINT8 [Peg2MaxLinkSpeed](#)  
*Offset 0x022C - PEG 2 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.*
  - UINT8 [Peg0MaxLinkWidth](#)  
*Offset 0x022D - PEG 0 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2, (0x3):Limit Link to x4, (0x4): Limit Link to x8 0:Auto, 1:x1, 2:x2, 3:x4, 4:x8.*
  - UINT8 [Peg1MaxLinkWidth](#)  
*Offset 0x022E - PEG 1 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2, (0x3):Limit Link to x4 0:Auto, 1:x1, 2:x2, 3:x4.*
  - UINT8 [Peg2MaxLinkWidth](#)  
*Offset 0x022F - PEG 2 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2 0:Auto, 1:x1, 2:x2.*
-

- UINT8 [Peg0PowerDownUnusedLanes](#)  
*Offset 0x0230 - Power down unused lanes on PEG 0 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.*
  - UINT8 [Peg1PowerDownUnusedLanes](#)  
*Offset 0x0231 - Power down unused lanes on PEG 1 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.*
  - UINT8 [Peg2PowerDownUnusedLanes](#)  
*Offset 0x0232 - Power down unused lanes on PEG 2 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.*
  - UINT8 [InitPcieAspmAfterOprom](#)  
*Offset 0x0233 - PCIe ASPM programming will happen in relation to the Oprom Select when PCIe ASPM programming will happen in relation to the Oprom.*
  - UINT8 [PegDisableSpreadSpectrumClocking](#)  
*Offset 0x0234 - PCIe Disable Spread Spectrum Clocking PCIe Disable Spread Spectrum Clocking.*
  - UINT8 [DmiGen3RootPortPreset](#) [4]  
*Offset 0x0235 - DMI Gen3 Root port preset values per lane Used for programming DMI Gen3 preset values per lane.*
  - UINT8 [DmiGen3EndPointPreset](#) [4]  
*Offset 0x0239 - DMI Gen3 End port preset values per lane Used for programming DMI Gen3 preset values per lane.*
  - UINT8 [DmiGen3EndPointHint](#) [4]  
*Offset 0x023D - DMI Gen3 End port Hint values per lane Used for programming DMI Gen3 Hint values per lane.*
  - UINT8 [DmiGen3RxCtlPeaking](#) [2]  
*Offset 0x0241 - DMI Gen3 RxCTLEp per-Bundle control Range: 0-15, 3 is default for each bundle, must be specified based upon platform design.*
  - UINT8 [DmiDeEmphasis](#)  
*Offset 0x0243 - DeEmphasis control for DMI DeEmphasis control for DMI.*
  - UINT8 [PegGen3RxCtlPeaking](#) [8]  
*Offset 0x0244 - PEG Gen3 RxCTLEp per-Bundle control Range: 0-15, 12 is default for each bundle, must be specified based upon platform design.*
  - UINT32 [PegDataPtr](#)  
*Offset 0x024C - Memory data pointer for saved preset search results The reference code will store the Gen3 Preset Search results in the SaDataHob's PegData structure (SA\_PEG\_DATA) and platform code can save/restore this data to skip preset search in the following boots.*
  - UINT8 [PegGpioData](#) [16]  
*Offset 0x0250 - PEG PERST# GPIO information The reference code will use the information in this structure in order to reset PCIe Gen3 devices during equalization, if necessary.*
  - UINT8 [UnusedUpdSpace7](#) [1]  
*Offset 0x0260.*
  - UINT8 [PegRootPortHPE](#) [3]  
*Offset 0x0261 - PCIe Hot Plug Enable/Disable per port 0(Default): Disable, 1: Enable.*
  - UINT32 [GttMmAdr](#)  
*Offset 0x0264 - Temporary MMIO address for GTTMADR The reference code will use the information in this structure in order to reset PCIe Gen3 devices during equalization, if necessary.*
  - UINT16 [GttSize](#)  
*Offset 0x0268 - Selection of iGFX GTT Memory size 1=2MB, 2=4MB, 3=8MB, Default is 3 1:2MB, 2:4MB, 3:8MB.*
  - UINT8 [PrimaryDisplay](#)  
*Offset 0x026A - Selection of the primary display device 0=iGFX, 1=PEG, 2=PCIe Graphics on PCH, 3(Default)=A↔UTO, 4=Switchable Graphics 0:iGFX, 1:PEG, 2:PCIe Graphics on PCH, 3:AUTO, 4:Switchable Graphics.*
  - UINT8 [SaRtd3Pcie0Gpio](#) [24]  
*Offset 0x026B - Switchable Graphics GPIO information for PEG 0 Switchable Graphics GPIO information for PEG 0, for Reset, power and wake GPIOs.*
  - UINT8 [SaRtd3Pcie1Gpio](#) [24]  
*Offset 0x0283 - Switchable Graphics GPIO information for PEG 1 Switchable Graphics GPIO information for PEG 1, for Reset, power and wake GPIOs.*
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- UINT8 [SaRtd3Pcie2Gpio](#) [24]  
*Offset 0x029B - Switchable Graphics GPIO information for PEG 2 Switchable Graphics GPIO information for PEG 2, for Reset, power and wake GPIOs.*
  - UINT8 [RootPortDev](#)  
*Offset 0x02B3 - PEG root port Device number for Switchable Graphics dGPU Device number to indicate which PEG root port has dGPU.*
  - UINT8 [RootPortFun](#)  
*Offset 0x02B4 - PEG root port Function number for Switchable Graphics dGPU Function number to indicate which PEG root port has dGPU.*
  - UINT8 [TxtImplemented](#)  
*Offset 0x02B5 - Enable/Disable MRC TXT dependency When enabled MRC execution will wait for TXT initialization to be done first.*
  - UINT8 [SaOcSupport](#)  
*Offset 0x02B6 - Enable/Disable SA OcSupport Enable: Enable SA OcSupport, Disable(Default): Disable SA OcSupport \$EN\_DIS.*
  - UINT8 [GtsVoltageMode](#)  
*Offset 0x02B7 - GT slice Voltage Mode 0(Default): Adaptive, 1: Override 0: Adaptive, 1: Override.*
  - UINT8 [GtusVoltageMode](#)  
*Offset 0x02B8 - GT unslice Voltage Mode 0(Default): Adaptive, 1: Override 0: Adaptive, 1: Override.*
  - UINT8 [GtsMaxOcRatio](#)  
*Offset 0x02B9 - Maximum GTs turbo ratio override 0(Default)=Minimal/Auto, 60=Maximum.*
  - UINT16 [GtsVoltageOffset](#)  
*Offset 0x02BA - The voltage offset applied to GT slice 0(Default)=Minimal, 1000=Maximum.*
  - UINT16 [GtsVoltageOverride](#)  
*Offset 0x02BC - The GT slice voltage override which is applied to the entire range of GT frequencies 0(Default)=Minimal, 2000=Maximum.*
  - UINT16 [GtsExtraTurboVoltage](#)  
*Offset 0x02BE - adaptive voltage applied during turbo frequencies 0(Default)=Minimal, 2000=Maximum.*
  - UINT16 [GtusVoltageOffset](#)  
*Offset 0x02C0 - voltage offset applied to GT unslice 0(Default)=Minimal, 2000=Maximum.*
  - UINT16 [GtusVoltageOverride](#)  
*Offset 0x02C2 - GT unslice voltage override which is applied to the entire range of GT frequencies 0(Default)=Minimal, 2000=Maximum.*
  - UINT16 [GtusExtraTurboVoltage](#)  
*Offset 0x02C4 - adaptive voltage applied during turbo frequencies 0(Default)=Minimal, 2000=Maximum.*
  - UINT16 [SaVoltageOffset](#)  
*Offset 0x02C6 - voltage offset applied to the SA 0(Default)=Minimal, 1000=Maximum.*
  - UINT8 [EdramRatio](#)  
*Offset 0x02C8 - EDram ratio override EdramRatio is deprecated on Kabylake.*
  - UINT8 [GtusMaxOcRatio](#)  
*Offset 0x02C9 - Maximum GTus turbo ratio override 0(Default)=Minimal, 60=Maximum.*
  - UINT8 [BistOnReset](#)  
*Offset 0x02CA - BIST on Reset Enable or Disable BIST on Reset; **0: Disable**; 1: Enable.*
  - UINT8 [SkipStopPbet](#)  
*Offset 0x02CB - Skip Stop PBET Timer Enable/Disable Skip Stop PBET Timer; **0: Disable**; 1: Enable \$EN\_DIS.*
  - UINT8 [EnableC6Dram](#)  
*Offset 0x02CC - C6DRAM power gating feature This feature is not supported.*
  - UINT8 [OcSupport](#)  
*Offset 0x02CD - Over clocking support Over clocking support; **0: Disable**; 1: Enable \$EN\_DIS.*
  - UINT8 [OcLock](#)  
*Offset 0x02CE - Over clocking Lock Over clocking Lock Enable/Disable; 0: Disable; **1: Enable** \$EN\_DIS.*
  - UINT8 [CoreMaxOcRatio](#)
-

Offset 0x02CF - Maximum Core Turbo Ratio Override Maximum core turbo ratio override allows to increase CPU core frequency beyond the fused max turbo ratio limit.

- UINT8 [CoreVoltageMode](#)

Offset 0x02D0 - Core voltage mode Core voltage mode; **0: Adaptive**; 1: Override.

- UINT8 [RingMinOcRatio](#)

Offset 0x02D1 - Minimum clr turbo ratio override Minimum clr turbo ratio override.

- UINT8 [RingMaxOcRatio](#)

Offset 0x02D2 - Maximum clr turbo ratio override Maximum clr turbo ratio override allows to increase CPU clr frequency beyond the fused max turbo ratio limit.

- UINT8 [HyperThreading](#)

Offset 0x02D3 - Hyper Threading Enable/Disable Enable or Disable Hyper Threading; 0: Disable; **1: Enable** \$EN←\_DIS.

- UINT8 [CpuRatioOverride](#)

Offset 0x02D4 - Enable or Disable CPU Ratio Override Enable or Disable CPU Ratio Override; **0: Disable**; 1: Enable.

- UINT8 [CpuRatio](#)

Offset 0x02D5 - CPU ratio value CPU ratio value.

- UINT8 [BootFrequency](#)

Offset 0x02D6 - Boot frequency Sets the boot frequency starting from reset vector.

- UINT8 [ActiveCoreCount](#)

Offset 0x02D7 - Number of active cores Number of active cores(Depends on Number of cores).

- UINT8 [FClkFrequency](#)

Offset 0x02D8 - Processor Early Power On Configuration FCLK setting **0: 800 MHz (ULT/ULX)**.

- UINT8 [JtagC10PowerGateDisable](#)

Offset 0x02D9 - Power JTAG in C10 and deeper power states Power JTAG in C10 and deeper power states; **0: Disable**; 1: Enable.

- UINT8 [VmxEnable](#)

Offset 0x02DA - Enable or Disable VMX Enable or Disable VMX; 0: Disable; **1: Enable**.

- UINT8 [Avx2RatioOffset](#)

Offset 0x02DB - AVX2 Ratio Offset 0(Default)= No Offset.

- UINT16 [CoreVoltageOverride](#)

Offset 0x02DC - core voltage override The core voltage override which is applied to the entire range of cpu core frequencies.

- UINT16 [CoreVoltageAdaptive](#)

Offset 0x02DE - Core Turbo voltage Adaptive Extra Turbo voltage applied to the cpu core when the cpu is operating in turbo mode.

- UINT16 [CoreVoltageOffset](#)

Offset 0x02E0 - Core Turbo voltage Offset The voltage offset applied to the core while operating in turbo mode. Valid Range 0 to 1000.

- UINT8 [CorePllVoltageOffset](#)

Offset 0x02E2 - Core PLL voltage offset Core PLL voltage offset.

- UINT8 [RingDownBin](#)

Offset 0x02E3 - Ring Downbin Ring Downbin enable/disable.

- UINT8 [BclkAdaptiveVoltage](#)

Offset 0x02E4 - BCLK Adaptive Voltage Enable When enabled, the CPU V/F curves are aware of BCLK frequency when calculated.

- UINT8 [BiosGuard](#)

Offset 0x02E5 - BiosGuard Enable/Disable.

- UINT8 [EnableSgx](#)

Offset 0x02E6 - EnableSgx Enable/Disable.

- UINT8 [Txt](#)

Offset 0x02E7 - Txt Enable/Disable.

- UINT32 [PrmrrSize](#)



- Offset 0x02E8 - PrmrSize Enable/Disable.
  - UINT32 [SinitMemorySize](#)
    - Offset 0x02EC - SinitMemorySize Enable/Disable.
  - UINT64 [TxtDprMemoryBase](#)
    - Offset 0x02F0 - TxtDprMemoryBase Enable/Disable.
  - UINT32 [TxtDprMemorySize](#)
    - Offset 0x02F8 - TxtDprMemorySize Enable/Disable.
  - UINT32 [TxtHeapMemorySize](#)
    - Offset 0x02FC - TxtHeapMemorySize Enable/Disable.
  - UINT8 [FlashWearOutProtection](#)
    - Offset 0x0300 - FlashWearOutProtection Enable/Disable.
  - UINT8 [TvbRatioClipping](#)
    - Offset 0x0301 - Thermal Velocity Boost Ratio clipping 0(Default): Disabled, 1: Enabled.
  - UINT8 [TvbVoltageOptimization](#)
    - Offset 0x0302 - Thermal Velocity Boost voltage optimization 0: Disabled, 1: Enabled(Default).
  - UINT8 [ReservedSecurityPreMem](#) [7]
    - Offset 0x0303 - ReservedSecurityPreMem Reserved for Security Pre-Mem \$EN\_DIS.
  - UINT8 [PchHpetEnable](#)
    - Offset 0x030A - PCH HPET Enabled Enable/disable PCH HPET.
  - UINT8 [PchHpetBdfValid](#)
    - Offset 0x030B - PCH HPET BDF valid Whether the BDF value is valid.
  - UINT32 [PchHpetBase](#)
    - Offset 0x030C - The HPET Base Address The HPET base address.
  - UINT8 [PchHpetBusNumber](#)
    - Offset 0x0310 - PCH HPET Bus Number Bus Number HPETn used as Requestor / Completer ID.
  - UINT8 [PchHpetDeviceNumber](#)
    - Offset 0x0311 - PCH HPET Device Number Device Number HPETn used as Requestor / Completer ID.
  - UINT8 [PchHpetFunctionNumber](#)
    - Offset 0x0312 - PCH HPET Function Number Function Number HPETn used as Requestor / Completer ID.
  - UINT8 [PchPcieHsioRxSetCtleEnable](#) [24]
    - Offset 0x0313 - Enable PCH HSIO PCIE Rx Set Ctle Enable PCH PCIE Gen 3 Set CTLE Value.
  - UINT8 [PchPcieHsioRxSetCtle](#) [24]
    - Offset 0x032B - PCH HSIO PCIE Rx Set Ctle Value PCH PCIE Gen 3 Set CTLE Value.
  - UINT8 [PchPcieHsioTxGen1DownscaleAmpEnable](#) [24]
    - Offset 0x0343 - Enble PCH HSIO PCIE TX Gen 1 Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchPcieHsioTxGen1DownscaleAmp](#) [24]
    - Offset 0x035B - PCH HSIO PCIE Gen 2 TX Output Downscale Amplitude Adjustment value PCH PCIE Gen 2 TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchPcieHsioTxGen2DownscaleAmpEnable](#) [24]
    - Offset 0x0373 - Enable PCH HSIO PCIE TX Gen 2 Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchPcieHsioTxGen2DownscaleAmp](#) [24]
    - Offset 0x038B - PCH HSIO PCIE Gen 2 TX Output Downscale Amplitude Adjustment value PCH PCIE Gen 2 TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchPcieHsioTxGen3DownscaleAmpEnable](#) [24]
    - Offset 0x03A3 - Enable PCH HSIO PCIE TX Gen 3 Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchPcieHsioTxGen3DownscaleAmp](#) [24]
    - Offset 0x03BB - PCH HSIO PCIE Gen 3 TX Output Downscale Amplitude Adjustment value PCH PCIE Gen 3 TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchPcieHsioTxGen1DeEmphEnable](#) [24]
-



- Offset 0x03D3 - Enable PCH HSIO PCIE Gen 1 TX Output De-Emphasis Adjustment Setting value override 0↔ : Disable; 1: Enable.
- UINT8 [PchPcieHsioTxGen1DeEmph](#) [24]
 

Offset 0x03EB - PCH HSIO PCIE Gen 1 TX Output De-Emphasis Adjustment value PCH PCIe Gen 1 TX Output De-Emphasis Adjustment Setting.
  - UINT8 [PchPcieHsioTxGen2DeEmph3p5Enable](#) [24]
 

Offset 0x0403 - Enable PCH HSIO PCIE Gen 2 TX Output -3.5dB De-Emphasis Adjustment Setting value override 0: Disable; 1: Enable.
  - UINT8 [PchPcieHsioTxGen2DeEmph3p5](#) [24]
 

Offset 0x041B - PCH HSIO PCIE Gen 2 TX Output -3.5dB De-Emphasis Adjustment value PCH PCIe Gen 2 TX Output -3.5dB De-Emphasis Adjustment Setting.
  - UINT8 [PchPcieHsioTxGen2DeEmph6p0Enable](#) [24]
 

Offset 0x0433 - Enable PCH HSIO PCIE Gen 2 TX Output -6.0dB De-Emphasis Adjustment Setting value override 0: Disable; 1: Enable.
  - UINT8 [PchPcieHsioTxGen2DeEmph6p0](#) [24]
 

Offset 0x044B - PCH HSIO PCIE Gen 2 TX Output -6.0dB De-Emphasis Adjustment value PCH PCIe Gen 2 TX Output -6.0dB De-Emphasis Adjustment Setting.
  - UINT8 [PchSataHsioRxGen1EqBoostMagEnable](#) [8]
 

Offset 0x0463 - Enable PCH HSIO SATA Receiver Equalization Boost Magnitude Adjustment Value override 0↔ : Disable; 1: Enable.
  - UINT8 [PchSataHsioRxGen1EqBoostMag](#) [8]
 

Offset 0x046B - PCH HSIO SATA 1.5 Gb/s Receiver Equalization Boost Magnitude Adjustment value PCH HSIO SATA 1.5 Gb/s Receiver Equalization Boost Magnitude Adjustment value.
  - UINT8 [PchSataHsioRxGen2EqBoostMagEnable](#) [8]
 

Offset 0x0473 - Enable PCH HSIO SATA Receiver Equalization Boost Magnitude Adjustment Value override 0↔ : Disable; 1: Enable.
  - UINT8 [PchSataHsioRxGen2EqBoostMag](#) [8]
 

Offset 0x047B - PCH HSIO SATA 3.0 Gb/s Receiver Equalization Boost Magnitude Adjustment value PCH HSIO SATA 3.0 Gb/s Receiver Equalization Boost Magnitude Adjustment value.
  - UINT8 [PchSataHsioRxGen3EqBoostMagEnable](#) [8]
 

Offset 0x0483 - Enable PCH HSIO SATA Receiver Equalization Boost Magnitude Adjustment Value override 0↔ : Disable; 1: Enable.
  - UINT8 [PchSataHsioRxGen3EqBoostMag](#) [8]
 

Offset 0x048B - PCH HSIO SATA 6.0 Gb/s Receiver Equalization Boost Magnitude Adjustment value PCH HSIO SATA 6.0 Gb/s Receiver Equalization Boost Magnitude Adjustment value.
  - UINT8 [PchSataHsioTxGen1DownscaleAmpEnable](#) [8]
 

Offset 0x0493 - Enable PCH HSIO SATA 1.5 Gb/s TX Output Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchSataHsioTxGen1DownscaleAmp](#) [8]
 

Offset 0x049B - PCH HSIO SATA 1.5 Gb/s TX Output Downscale Amplitude Adjustment value PCH HSIO SATA 1.5 Gb/s TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchSataHsioTxGen2DownscaleAmpEnable](#) [8]
 

Offset 0x04A3 - Enable PCH HSIO SATA 3.0 Gb/s TX Output Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchSataHsioTxGen2DownscaleAmp](#) [8]
 

Offset 0x04AB - PCH HSIO SATA 3.0 Gb/s TX Output Downscale Amplitude Adjustment value PCH HSIO SATA 3.0 Gb/s TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchSataHsioTxGen3DownscaleAmpEnable](#) [8]
 

Offset 0x04B3 - Enable PCH HSIO SATA 6.0 Gb/s TX Output Downscale Amplitude Adjustment value override 0: Disable; 1: Enable.
  - UINT8 [PchSataHsioTxGen3DownscaleAmp](#) [8]
 

Offset 0x04BB - PCH HSIO SATA 6.0 Gb/s TX Output Downscale Amplitude Adjustment value PCH HSIO SATA 6.0 Gb/s TX Output Downscale Amplitude Adjustment value.
  - UINT8 [PchSataHsioTxGen1DeEmphEnable](#) [8]
-

- Offset 0x04C3 - Enable PCH HSIO SATA 1.5 Gb/s TX Output De-Emphasis Adjustment Setting value override 0: Disable; 1: Enable.
- UINT8 [PchSataHsioTxGen1DeEmph](#) [8]
 

Offset 0x04CB - PCH HSIO SATA 1.5 Gb/s TX Output De-Emphasis Adjustment Setting PCH HSIO SATA 1.5 Gb/s TX Output De-Emphasis Adjustment Setting.
  - UINT8 [PchSataHsioTxGen2DeEmphEnable](#) [8]
 

Offset 0x04D3 - Enable PCH HSIO SATA 3.0 Gb/s TX Output De-Emphasis Adjustment Setting value override 0: Disable; 1: Enable.
  - UINT8 [PchSataHsioTxGen2DeEmph](#) [8]
 

Offset 0x04DB - PCH HSIO SATA 3.0 Gb/s TX Output De-Emphasis Adjustment Setting PCH HSIO SATA 3.0 Gb/s TX Output De-Emphasis Adjustment Setting.
  - UINT8 [PchSataHsioTxGen3DeEmphEnable](#) [8]
 

Offset 0x04E3 - Enable PCH HSIO SATA 6.0 Gb/s TX Output De-Emphasis Adjustment Setting value override 0: Disable; 1: Enable.
  - UINT8 [PchSataHsioTxGen3DeEmph](#) [8]
 

Offset 0x04EB - PCH HSIO SATA 6.0 Gb/s TX Output De-Emphasis Adjustment Setting PCH HSIO SATA 6.0 Gb/s TX Output De-Emphasis Adjustment Setting.
  - UINT8 [PchLpcEnhancePort8xhDecoding](#)

Offset 0x04F3 - PCH LPC Enhance the port 8xh decoding Original LPC only decodes one byte of port 80h.
  - UINT16 [PchAcpiBase](#)

Offset 0x04F4 - PCH Acpi Base Power management I/O base address.
  - UINT8 [PchPort80Route](#)

Offset 0x04F6 - PCH Port80 Route Control where the Port 80h cycles are sent, 0: LPC; 1: PCI.
  - UINT8 [SmbusArpEnable](#)

Offset 0x04F7 - Enable SMBus ARP support Enable SMBus ARP support.
  - UINT16 [PchSmbusIoBase](#)

Offset 0x04F8 - SMBUS Base Address SMBUS Base Address (IO space).
  - UINT8 [PchNumRsvdSmbusAddresses](#)

Offset 0x04FA - Number of RsvdSmbusAddressTable.
  - UINT8 [UnusedUpdSpace8](#)

Offset 0x04FB.
  - UINT32 [RsvdSmbusAddressTablePtr](#)

Offset 0x04FC - Point of RsvdSmbusAddressTable Array of addresses reserved for non-ARP-capable SMBus devices.
  - UINT32 [TraceHubMemReg0Size](#)

Offset 0x0500 - Trace Hub Memory Region 0 Trace Hub Memory Region 0.
  - UINT32 [TraceHubMemReg1Size](#)

Offset 0x0504 - Trace Hub Memory Region 1 Trace Hub Memory Region 1.
  - UINT32 [PcieRpEnableMask](#)

Offset 0x0508 - Enable PCIE RP Mask Enable/disable PCIE Root Ports.
  - UINT8 [PcdDebugInterfaceFlags](#)

Offset 0x050C - Debug Interfaces Debug Interfaces.
  - UINT8 [PcdSerialIoUartNumber](#)

Offset 0x050D - SerialIoUart Number Selection Select SerialIoUart Controller for debug.
  - UINT8 [PcdIsaSerialUartBase](#)

Offset 0x050E - ISA Serial Base selection Select ISA Serial Base address.
  - UINT8 [PchPmPciePllSsc](#)

Offset 0x050F - PCH Pm Pcie Pll Ssc Specifies the Pcie Pll Spread Spectrum Percentage.
  - UINT8 [PeciC10Reset](#)

Offset 0x0510 - Enable or Disable Peci C10 Reset command Enable or Disable Peci C10 Reset command; 0: Disable; 1: Enable.
  - UINT8 [PeciSxReset](#)
-

Offset 0x0511 - Enable or Disable Peci Sx Reset command Enable or Disable Peci Sx Reset command; **0: Disable**; 1: Enable.

- UINT8 [PcdSerialDebugBaudRate](#)

Offset 0x0512 - PcdSerialDebugBaudRate Baud Rate for Serial Debug Messages.

- UINT8 [PcdSerialDebugLevel](#)

Offset 0x0513 - PcdSerialDebugLevel Serial Debug Message Level.

- UINT8 [EvLoader](#)

Offset 0x0514 - Enable or Disable EV Loader Enable or Disable EV Loader; **0: Disable**; 1: Enable.

- UINT8 [GtPllVoltageOffset](#)

Offset 0x0515 - GT PLL voltage offset Core PLL voltage offset.

- UINT8 [RingPllVoltageOffset](#)

Offset 0x0516 - Ring PLL voltage offset Core PLL voltage offset.

- UINT8 [SaPllVoltageOffset](#)

Offset 0x0517 - System Agent PLL voltage offset Core PLL voltage offset.

- UINT8 [McPllVoltageOffset](#)

Offset 0x0518 - Memory Controller PLL voltage offset Core PLL voltage offset.

- UINT8 [RealtimeMemoryTiming](#)

Offset 0x0519 - Realtime Memory Timing 0(Default): Disabled, 1: Enabled.

- UINT8 [Avx3RatioOffset](#)

Offset 0x051A - AVX3 Ratio Offset 0(Default)= No Offset.

- UINT8 [CleanMemory](#)

Offset 0x051B - Ask MRC to clear memory content Ask MRC to clear memory content **0: Do not Clear Memory**; 1: Clear Memory.

- UINT8 [TjMaxOffset](#)

Offset 0x051C - TjMax Offset TjMax offset.

- UINT8 [ReservedFspmUpd](#) [3]

Offset 0x051D.

### 8.4.1 Detailed Description

Fsp M Configuration.

Definition at line 57 of file FspmUpd.h.

### 8.4.2 Member Data Documentation

#### 8.4.2.1 UINT8 FSP\_M\_CONFIG::ActiveCoreCount

Offset 0x02D7 - Number of active cores Number of active cores(Depends on Number of cores).

**0: All**; 1: 1 ;2: 2 ;3: 3 0:All, 1:1, 2:2, 3:3

Definition at line 805 of file FspmUpd.h.

#### 8.4.2.2 UINT8 FSP\_M\_CONFIG::ApertureSize

Offset 0x00E5 - Aperture Size Select the Aperture Size.

0:128 MB, 1:256 MB, 2:512 MB

Definition at line 217 of file FspmUpd.h.

#### 8.4.2.3 UINT8 FSP\_M\_CONFIG::Avx2RatioOffset

Offset 0x02DB - AVX2 Ratio Offset 0(Default)= No Offset.

Range 0 - 31. Specifies number of bins to decrease AVX ratio vs. Core Ratio. Uses Mailbox MSR 0x150, cmd 0x1B.

Definition at line 830 of file FspmUpd.h.

#### 8.4.2.4 UINT8 FSP\_M\_CONFIG::Avx3RatioOffset

Offset 0x051A - AVX3 Ratio Offset 0(Default)= No Offset.

Range 0 - 31. Specifies number of bins to decrease AVX ratio vs. Core Ratio. Uses Mailbox MSR 0x150, cmd 0x1B.

Definition at line 1280 of file FspmUpd.h.

#### 8.4.2.5 UINT8 FSP\_M\_CONFIG::BclkAdaptiveVoltage

Offset 0x02E4 - BCLK Adaptive Voltage Enable When enabled, the CPU V/F curves are aware of BCLK frequency when calculated.

0: Disable; **1: Enable \$EN\_DIS**

Definition at line 866 of file FspmUpd.h.

#### 8.4.2.6 UINT8 FSP\_M\_CONFIG::BiosGuard

Offset 0x02E5 - BiosGuard Enable/Disable.

0: Disable, Enable/Disable BIOS Guard feature, 1: enable \$EN\_DIS

Definition at line 872 of file FspmUpd.h.

#### 8.4.2.7 UINT8 FSP\_M\_CONFIG::BistOnReset

Offset 0x02CA - BIST on Reset Enable or Disable BIST on Reset; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 725 of file FspmUpd.h.

#### 8.4.2.8 UINT8 FSP\_M\_CONFIG::BootFrequency

Offset 0x02D6 - Boot frequency Sets the boot frequency starting from reset vector.

- 0: Maximum battery performance.- **1: Maximum non-turbo performance.**- 2: Turbo performance.

##### Note

If Turbo is selected BIOS will start in max non-turbo mode and switch to Turbo mode. 0:0, 1:1, 2:2

Definition at line 798 of file FspmUpd.h.

#### 8.4.2.9 UINT8 FSP\_M\_CONFIG::CleanMemory

Offset 0x051B - Ask MRC to clear memory content Ask MRC to clear memory content **0: Do not Clear Memory**; 1: Clear Memory.

\$EN\_DIS

Definition at line 1286 of file FspmUpd.h.

#### 8.4.2.10 UINT8 FSP\_M\_CONFIG::CmdTriStateDis

Offset 0x0191 - Command Tristate Support Enable/Disable Command Tristate; **0: Enable**; 1: Disable.

\$EN\_DIS

Definition at line 395 of file FspmUpd.h.

#### 8.4.2.11 UINT8 FSP\_M\_CONFIG::CoreMaxOcRatio

Offset 0x02CF - Maximum Core Turbo Ratio Override Maximum core turbo ratio override allows to increase CPU core frequency beyond the fused max turbo ratio limit.

**0: Hardware defaults.** Range: 0-255

Definition at line 755 of file FspmUpd.h.

#### 8.4.2.12 UINT8 FSP\_M\_CONFIG::CorePllVoltageOffset

Offset 0x02E2 - Core PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line 852 of file FspmUpd.h.

#### 8.4.2.13 UINT16 FSP\_M\_CONFIG::CoreVoltageAdaptive

Offset 0x02DE - Core Turbo voltage Adaptive Extra Turbo voltage applied to the cpu core when the cpu is operating in turbo mode.

Valid Range 0 to 2000

Definition at line 842 of file FspmUpd.h.

#### 8.4.2.14 UINT8 FSP\_M\_CONFIG::CoreVoltageMode

Offset 0x02D0 - Core voltage mode Core voltage mode; **0: Adaptive**; 1: Override.

\$EN\_DIS

Definition at line 761 of file FspmUpd.h.

#### 8.4.2.15 UINT16 FSP\_M\_CONFIG::CoreVoltageOverride

Offset 0x02DC - core voltage override The core voltage override which is applied to the entire range of cpu core frequencies.

Valid Range 0 to 2000

Definition at line 836 of file FspmUpd.h.

#### 8.4.2.16 UINT8 FSP\_M\_CONFIG::CpuRatio

Offset 0x02D5 - CPU ratio value CPU ratio value.

Valid Range 0 to 63

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Definition at line 790 of file FspmUpd.h.

#### 8.4.2.17 UINT8 FSP\_M\_CONFIG::CpuRatioOverride

Offset 0x02D4 - Enable or Disable CPU Ratio Override Enable or Disable CPU Ratio Override; **0: Disable**; 1: Enable.

##### Note

If disabled, BIOS will use the default max non-turbo ratio, and will not use any flex ratio setting. \$EN\_DIS

Definition at line 785 of file FspmUpd.h.

#### 8.4.2.18 UINT16 FSP\_M\_CONFIG::DdrFreqLimit

Offset 0x00E8 - DDR Frequency Limit Maximum Memory Frequency Selections in Mhz.

Options are 1067, 1333, 1600, 1867, 2133, 2400 and 0 for Auto. 1067:1067, 1333:1333, 1600:1600, 1867:1867, 2133:2133, 2400:2400, 0:Auto

Definition at line 238 of file FspmUpd.h.

#### 8.4.2.19 UINT8 FSP\_M\_CONFIG::DmiDeEmphasis

Offset 0x0243 - DeEmphasis control for DMI DeEmphasis control for DMI.

0=-6dB, 1(Default)=-3.5 dB 0: -6dB, 1: -3.5dB

Definition at line 574 of file FspmUpd.h.

#### 8.4.2.20 UINT8 FSP\_M\_CONFIG::DmiGen3EndPointHint[4]

Offset 0x023D - DMI Gen3 End port Hint values per lane Used for programming DMI Gen3 Hint values per lane.

Range: 0-6, 2 is default for each lane

Definition at line 563 of file FspmUpd.h.

#### 8.4.2.21 UINT8 FSP\_M\_CONFIG::DmiGen3EndPointPreset[4]

Offset 0x0239 - DMI Gen3 End port preset values per lane Used for programming DMI Gen3 preset values per lane.

Range: 0-9, 7 is default for each lane

Definition at line 558 of file FspmUpd.h.

#### 8.4.2.22 UINT8 FSP\_M\_CONFIG::DmiGen3ProgramStaticEq

Offset 0x0226 - Enable/Disable DMI GEN3 Static EQ Phase1 programming Program DMI Gen3 EQ Phase1 Static Presets.

Disabled(0x0): Disable EQ Phase1 Static Presets Programming, Enabled(0x1)(Default): Enable EQ Phase1 Static Presets Programming \$EN\_DIS

Definition at line 449 of file FspmUpd.h.

#### 8.4.2.23 UINT8 FSP\_M\_CONFIG::DmiGen3RootPortPreset[4]

Offset 0x0235 - DMI Gen3 Root port preset values per lane Used for programming DMI Gen3 preset values per lane.

Range: 0-9, 4 is default for each lane

Definition at line 553 of file FspmUpd.h.

#### 8.4.2.24 UINT8 FSP\_M\_CONFIG::DpSscMarginEnable

Offset 0x00A7 - DpSscMarginEnable Enable/Disable.

0: Disable, Use default DisplayPort SSC modulation range 0.5% down spread, 1: Enable DisplayPort SSC range reduction. Note this should only be used on systems that exceeds allowed SSC modulation range as defined in VESA's spec \$EN\_DIS

Definition at line 195 of file FspmUpd.h.

#### 8.4.2.25 UINT8 FSP\_M\_CONFIG::EnableC6Dram

Offset 0x02CC - C6DRAM power gating feature This feature is not supported.

BIOS is required to disable. **0: Disable** \$EN\_DIS

Definition at line 737 of file FspmUpd.h.

#### 8.4.2.26 UINT8 FSP\_M\_CONFIG::EnableSgx

Offset 0x02E6 - EnableSgx Enable/Disable.

0: Disable, Enable/Disable SGX feature, 1: enable \$EN\_DIS

Definition at line 878 of file FspmUpd.h.

#### 8.4.2.27 UINT8 FSP\_M\_CONFIG::EnableTraceHub

Offset 0x00A6 - Enable Trace Hub Enable/disable Trace Hub function.

\$EN\_DIS

Definition at line 187 of file FspmUpd.h.

#### 8.4.2.28 UINT8 FSP\_M\_CONFIG::EvLoader

Offset 0x0514 - Enable or Disable EV Loader Enable or Disable EV Loader; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 1243 of file FspmUpd.h.

#### 8.4.2.29 UINT8 FSP\_M\_CONFIG::FclkFrequency

Offset 0x02D8 - Processor Early Power On Configuration FCLK setting **0: 800 MHz (ULT/ULX)**.

**1: 1 GHz (DT/Halo)**. Not supported on ULT/ULX.- 2: 400 MHz. - 3: Reserved 0:800 MHz, 1: 1 GHz, 2: 400 MHz, 3: Reserved

Definition at line 812 of file FspmUpd.h.

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#### 8.4.2.30 UINT8 FSP\_M\_CONFIG::FlashWearOutProtection

Offset 0x0300 - FlashWearOutProtection Enable/Disable.

0: Disable, Enable/Disable FlashWearOutProtection feature, 1: enable \$EN\_DIS

Definition at line 915 of file FspmUpd.h.

#### 8.4.2.31 UINT8 FSP\_M\_CONFIG::GtPllVoltageOffset

Offset 0x0515 - GT PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63 0x0:0xFF

Definition at line 1249 of file FspmUpd.h.

#### 8.4.2.32 UINT8 FSP\_M\_CONFIG::HeciTimeouts

Offset 0x01AC - HECI Timeouts Enable/Disable.

0: Disable, disable timeout check for HECI, 1: enable \$EN\_DIS

Definition at line 420 of file FspmUpd.h.

#### 8.4.2.33 UINT8 FSP\_M\_CONFIG::IgdDvmt50PreAlloc

Offset 0x00E3 - Internal Graphics Pre-allocated Memory Size of memory preallocated for internal graphics.

0x00:0 MB, 0x01:32 MB, 0x02:64 MB

Definition at line 205 of file FspmUpd.h.

#### 8.4.2.34 UINT8 FSP\_M\_CONFIG::InitPcieAspmAfterOprom

Offset 0x0233 - PCIe ASPM programming will happen in relation to the Oprom Select when PCIe ASPM programming will happen in relation to the Oprom.

Before(0x0)(Default): Do PCIe ASPM programming before Oprom, After(0x1): Do PCIe ASPM programming after Oprom, requires an SMI handler to save/restore ASPM settings during S3 resume 0:Before, 1:After

Definition at line 541 of file FspmUpd.h.

#### 8.4.2.35 UINT8 FSP\_M\_CONFIG::InternalGfx

Offset 0x00E4 - Internal Graphics Enable/disable internal graphics.

\$EN\_DIS

Definition at line 211 of file FspmUpd.h.

#### 8.4.2.36 UINT8 FSP\_M\_CONFIG::JtagC10PowerGateDisable

Offset 0x02D9 - Power JTAG in C10 and deeper power states Power JTAG in C10 and deeper power states; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 818 of file FspmUpd.h.

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**8.4.2.37** `UINT8 FSP_M_CONFIG::McPllVoltageOffset`

Offset 0x0518 - Memory Controller PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63 0x0:0xFF

Definition at line 1267 of file FspmUpd.h.

**8.4.2.38** `UINT16 FSP_M_CONFIG::MmioSize`

Offset 0x00A0 - MMIO Size Size of MMIO space reserved for devices.

0(Default)=Auto, non-Zero=size in MB

Definition at line 164 of file FspmUpd.h.

**8.4.2.39** `UINT8 FSP_M_CONFIG::PcdDebugInterfaceFlags`

Offset 0x050C - Debug Interfaces Debug Interfaces.

BIT0-RAM, BIT1-UART, BIT3-USB3, BIT4-Serial IO, BIT5-TraceHub, BIT2 - Not used.

Definition at line 1192 of file FspmUpd.h.

**8.4.2.40** `UINT8 FSP_M_CONFIG::PcdIsaSerialUartBase`

Offset 0x050E - ISA Serial Base selection Select ISA Serial Base address.

Default is 0x3F8. 0:0x3F8, 1:0x2F8

Definition at line 1204 of file FspmUpd.h.

**8.4.2.41** `UINT8 FSP_M_CONFIG::PcdSerialDebugBaudRate`

Offset 0x0512 - PcdSerialDebugBaudRate Baud Rate for Serial Debug Messages.

3:9600, 4:19200, 6:56700, 7:115200. 3:9600, 4:19200, 6:56700, 7:115200

Definition at line 1228 of file FspmUpd.h.

**8.4.2.42** `UINT8 FSP_M_CONFIG::PcdSerialDebugLevel`

Offset 0x0513 - PcdSerialDebugLevel Serial Debug Message Level.

0:Disable, 1>Error Only, 2>Error & Warnings, 3:Load, Error, Warnings & Info, 4:Load, Error, Warnings, Info & Event, 5:Load, Error, Warnings, Info & Verbose 0:Disable, 1>Error Only, 2>Error and Warnings, 3:Load Error Warnings and Info, 4:Load Error Warnings and Info, 5:Load Error Warnings Info and Verbose

Definition at line 1237 of file FspmUpd.h.

**8.4.2.43** `UINT8 FSP_M_CONFIG::PcdSerialUartNumber`

Offset 0x050D - SerialUart Number Selection Select SerialUart Controller for debug.

0:SerialUart0, 1:SerialUart1, 2:SerialUart2

Definition at line 1198 of file FspmUpd.h.

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**8.4.2.44 UINT16 FSP\_M\_CONFIG::PchAcpiBase**

Offset 0x04F4 - PCH Acpi Base Power management I/O base address.

Default is 0x1800.

Definition at line 1139 of file FspmUpd.h.

**8.4.2.45 UINT32 FSP\_M\_CONFIG::PchHpetBase**

Offset 0x030C - The HPET Base Address The HPET base address.

Default is 0xFED00000.

Definition at line 953 of file FspmUpd.h.

**8.4.2.46 UINT8 FSP\_M\_CONFIG::PchHpetBdfValid**

Offset 0x030B - PCH HPET BDF valid Whether the BDF value is valid.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line 948 of file FspmUpd.h.

**8.4.2.47 UINT8 FSP\_M\_CONFIG::PchHpetBusNumber**

Offset 0x0310 - PCH HPET Bus Number Bus Number HPETn used as Requestor / Completer ID.

Default is 0xF0.

Definition at line 958 of file FspmUpd.h.

**8.4.2.48 UINT8 FSP\_M\_CONFIG::PchHpetDeviceNumber**

Offset 0x0311 - PCH HPET Device Number Device Number HPETn used as Requestor / Completer ID.

Default is 0x1F.

Definition at line 963 of file FspmUpd.h.

**8.4.2.49 UINT8 FSP\_M\_CONFIG::PchHpetEnable**

Offset 0x030A - PCH HPET Enabled Enable/disable PCH HPET.

\$EN\_DIS

Definition at line 942 of file FspmUpd.h.

**8.4.2.50 UINT8 FSP\_M\_CONFIG::PchHpetFunctionNumber**

Offset 0x0312 - PCH HPET Function Number Function Number HPETn used as Requestor / Completer ID.

Default is 0x00.

Definition at line 968 of file FspmUpd.h.

**8.4.2.51 UINT8 FSP\_M\_CONFIG::PchLpcEnhancePort8xhDecoding**

Offset 0x04F3 - PCH LPC Enhance the port 8xh decoding Original LPC only decodes one byte of port 80h.

\$EN\_DIS

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Definition at line 1134 of file FspmUpd.h.

#### 8.4.2.52 UINT8 FSP\_M\_CONFIG::PchNumRsvdSmbusAddresses

Offset 0x04FA - Number of RsvdSmbusAddressTable.

The number of elements in the RsvdSmbusAddressTable.

Definition at line 1161 of file FspmUpd.h.

#### 8.4.2.53 UINT8 FSP\_M\_CONFIG::PchPmPciePIISsc

Offset 0x050F - PCH Pm Pcie PII Ssc Specifies the Pcie PII Spread Spectrum Percentage.

The default is 0xFF: AUTO - No BIOS override.

Definition at line 1210 of file FspmUpd.h.

#### 8.4.2.54 UINT8 FSP\_M\_CONFIG::PchPort80Route

Offset 0x04F6 - PCH Port80 Route Control where the Port 80h cycles are sent, 0: LPC; 1: PCI.

\$EN\_DIS

Definition at line 1145 of file FspmUpd.h.

#### 8.4.2.55 UINT32 FSP\_M\_CONFIG::PcieRpEnableMask

Offset 0x0508 - Enable PCIE RP Mask Enable/disable PCIE Root Ports.

0: disable, 1: enable. One bit for each port, bit0 for port1, bit1 for port2, and so on.

Definition at line 1186 of file FspmUpd.h.

#### 8.4.2.56 UINT8 FSP\_M\_CONFIG::PeciC10Reset

Offset 0x0510 - Enable or Disable Peci C10 Reset command Enable or Disable Peci C10 Reset command; 0: Disable; **1: Enable.**

\$EN\_DIS

Definition at line 1216 of file FspmUpd.h.

#### 8.4.2.57 UINT8 FSP\_M\_CONFIG::PeciSxReset

Offset 0x0511 - Enable or Disable Peci Sx Reset command Enable or Disable Peci Sx Reset command; **0: Disable;** 1: Enable.

\$EN\_DIS

Definition at line 1222 of file FspmUpd.h.

#### 8.4.2.58 UINT32 FSP\_M\_CONFIG::PegDataPtr

Offset 0x024C - Memory data pointer for saved preset search results The reference code will store the Gen3 Preset Search results in the SaDataHob's PegData structure (SA\_PEG\_DATA) and platform code can save/restore this data to skip preset search in the following boots.

Range: 0-0xFFFFFFFF, default is 0

Definition at line 586 of file FspmUpd.h.

#### 8.4.2.59 UINT8 FSP\_M\_CONFIG::PegDisableSpreadSpectrumClocking

Offset 0x0234 - PCIe Disable Spread Spectrum Clocking PCIe Disable Spread Spectrum Clocking.

Normal Operation(0x0)(Default) - SSC enabled, Disable SSC(0X1) - Disable SSC per platform design or for compliance testing 0:Normal Operation, 1:Disable SSC

Definition at line 548 of file FspmUpd.h.

#### 8.4.2.60 UINT32 FSP\_M\_CONFIG::PrmrrSize

Offset 0x02E8 - PrmrrSize Enable/Disable.

0: Disable, define default value of PrmrrSize , 1: enable

Definition at line 889 of file FspmUpd.h.

#### 8.4.2.61 UINT8 FSP\_M\_CONFIG::ProbelessTrace

Offset 0x00A2 - Probeless Trace Probeless Trace: 0=Disabled, 1=Enable.

Enabling Probeless Trace will reserve 128MB. This also requires IED to be enabled. \$EN\_DIS

Definition at line 171 of file FspmUpd.h.

#### 8.4.2.62 UINT8 FSP\_M\_CONFIG::Ratio

Offset 0x017B - Memory Ratio Automatic or the frequency will equal ratio times reference clock.

Set to Auto to recalculate memory timings listed below. 0:Auto, 4:4, 5:5, 6:6, 7:7, 8:8, 9:9, 10:10, 11:11, 12:12, 13:13, 14:14, 15:15

Definition at line 301 of file FspmUpd.h.

#### 8.4.2.63 UINT8 FSP\_M\_CONFIG::RealtimeMemoryTiming

Offset 0x0519 - Realtime Memory Timing 0(Default): Disabled, 1: Enabled.

When enabled, it will allow the system to perform realtime memory timing changes after MRC\_DONE. 0: Disabled, 1: Enabled

Definition at line 1274 of file FspmUpd.h.

#### 8.4.2.64 UINT8 FSP\_M\_CONFIG::RefClk

Offset 0x017A - Memory Reference Clock Automatic, 100MHz, 133MHz.

0:Auto, 1:133MHz, 2:100MHz

Definition at line 294 of file FspmUpd.h.

#### 8.4.2.65 UINT8 FSP\_M\_CONFIG::RingDownBin

Offset 0x02E3 - Ring Downbin Ring Downbin enable/disable.

When enabled, CPU will ensure the ring ratio is always lower than the core ratio. 0: Disable; **1: Enable.** \$EN\_DIS

Definition at line 859 of file FspmUpd.h.

#### 8.4.2.66 UINT8 FSP\_M\_CONFIG::RingMaxOcRatio

Offset 0x02D2 - Maximum clr turbo ratio override Maximum clr turbo ratio override allows to increase CPU clr frequency beyond the fused max turbo ratio limit.

**0: Hardware defaults.** Range: 0-255

Definition at line 772 of file FspmUpd.h.

#### 8.4.2.67 UINT8 FSP\_M\_CONFIG::RingMinOcRatio

Offset 0x02D1 - Minimum clr turbo ratio override Minimum clr turbo ratio override.

**0: Hardware defaults.** Range: 0-255

Definition at line 766 of file FspmUpd.h.

#### 8.4.2.68 UINT8 FSP\_M\_CONFIG::RingPIIVoltageOffset

Offset 0x0516 - Ring PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63 0x0:0xFF

Definition at line 1255 of file FspmUpd.h.

#### 8.4.2.69 UINT8 FSP\_M\_CONFIG::RMT

Offset 0x00E7 - Rank Margin Tool Enable/disable Rank Margin Tool.

\$EN\_DIS

Definition at line 231 of file FspmUpd.h.

#### 8.4.2.70 UINT8 FSP\_M\_CONFIG::SaGv

Offset 0x00E6 - SA GV System Agent dynamic frequency support and when enabled memory will be training at two different frequencies.

Only effects ULX/ULT CPUs. 0=Disabled, 1=FixedLow, 2=FixedHigh, and 3=Enabled. 0:Disabled, 1:FixedLow, 2:FixedHigh, 3:Enabled

Definition at line 225 of file FspmUpd.h.

#### 8.4.2.71 UINT8 FSP\_M\_CONFIG::SaPIIVoltageOffset

Offset 0x0517 - System Agent PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63 0x0:0xFF

Definition at line 1261 of file FspmUpd.h.

#### 8.4.2.72 UINT32 FSP\_M\_CONFIG::SinitMemorySize

Offset 0x02EC - SinitMemorySize Enable/Disable.

0: Disable, define default value of SinitMemorySize , 1: enable

Definition at line 894 of file FspmUpd.h.

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#### 8.4.2.73 UINT8 FSP\_M\_CONFIG::SmbusArpEnable

Offset 0x04F7 - Enable SMBus ARP support Enable SMBus ARP support.

\$EN\_DIS

Definition at line 1151 of file FspmUpd.h.

#### 8.4.2.74 UINT8 FSP\_M\_CONFIG::SmbusEnable

Offset 0x00A5 - Enable SMBus Enable/disable SMBus controller.

\$EN\_DIS

Definition at line 181 of file FspmUpd.h.

#### 8.4.2.75 UINT8 FSP\_M\_CONFIG::SpdProfileSelected

Offset 0x0177 - SPD Profile Selected Select DIMM timing profile.

Options are 0=Default profile, 1=Custom profile, 2=XMP Profile 1, 3=XMP Profile 2 0:Default profile, 1:Custom profile, 2:XMP profile 1, 3:XMP profile 2

Definition at line 280 of file FspmUpd.h.

#### 8.4.2.76 UINT8 FSP\_M\_CONFIG::TjMaxOffset

Offset 0x051C - TjMax Offset TjMax offset.

Specified value here is clipped by pCode (125 - TjMax Offset) to support TjMax in the range of 62 to 115 deg Celsius. Valid Range 0 - 63

Definition at line 1292 of file FspmUpd.h.

#### 8.4.2.77 UINT8 FSP\_M\_CONFIG::tRTP

Offset 0x0189 - tRTP Min Internal Read to Precharge Command Delay Time, 0: AUTO, max: 15.

DDR4 legal values: 5, 6, 7, 8, 9, 10, 12

Definition at line 353 of file FspmUpd.h.

#### 8.4.2.78 UINT32 FSP\_M\_CONFIG::TsegSize

Offset 0x009C - Tseg Size Size of SMRAM memory reserved.

0x400000 for Release build and 0x1000000 for Debug build 0x0400000:4MB, 0x01000000:16MB

Definition at line 159 of file FspmUpd.h.

#### 8.4.2.79 UINT8 FSP\_M\_CONFIG::TvbRatioClipping

Offset 0x0301 - Thermal Velocity Boost Ratio clipping 0(Default): Disabled, 1: Enabled.

This service controls Core frequency reduction caused by high package temperatures for processors that implement the Intel Thermal Velocity Boost (TVB) feature 0: Disabled, 1: Enabled

Definition at line 923 of file FspmUpd.h.

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**8.4.2.80 UINT8 FSP\_M\_CONFIG::TvbVoltageOptimization**

Offset 0x0302 - Thermal Velocity Boost voltage optimization 0: Disabled, 1: Enabled(Default).

This service controls thermal based voltage optimizations for processors that implement the Intel Thermal Velocity Boost (TVB) feature. 0: Disabled, 1: Enabled

Definition at line 930 of file FspmUpd.h.

**8.4.2.81 UINT8 FSP\_M\_CONFIG::Txt**

Offset 0x02E7 - Txt Enable/Disable.

0: Disable, Enable/Disable Txt feature, 1: enable \$EN\_DIS

Definition at line 884 of file FspmUpd.h.

**8.4.2.82 UINT64 FSP\_M\_CONFIG::TxtDprMemoryBase**

Offset 0x02F0 - TxtDprMemoryBase Enable/Disable.

0: Disable, define default value of TxtDprMemoryBase , 1: enable

Definition at line 899 of file FspmUpd.h.

**8.4.2.83 UINT32 FSP\_M\_CONFIG::TxtDprMemorySize**

Offset 0x02F8 - TxtDprMemorySize Enable/Disable.

0: Disable, define default value of TxtDprMemorySize , 1: enable

Definition at line 904 of file FspmUpd.h.

**8.4.2.84 UINT32 FSP\_M\_CONFIG::TxtHeapMemorySize**

Offset 0x02FC - TxtHeapMemorySize Enable/Disable.

0: Disable, define default value of TxtHeapMemorySize , 1: enable

Definition at line 909 of file FspmUpd.h.

**8.4.2.85 UINT8 FSP\_M\_CONFIG::TxtImplemented**

Offset 0x02B5 - Enable/Disable MRC TXT dependency When enabled MRC execution will wait for TXT initialization to be done first.

Disabled(0x0)(Default): MRC will not wait for TXT initialization, Enabled(0x1): MRC will wait for TXT initialization \$EN\_DIS

Definition at line 651 of file FspmUpd.h.

**8.4.2.86 UINT16 FSP\_M\_CONFIG::VddVoltage**

Offset 0x0178 - Memory Voltage Memory Voltage Override (Vddq).

Default = no override 0:Default, 1100:1.10 Volts, 1150:1.15 Volts, 1200:1.20 Volts, 1250:1.25 Volts, 1300:1.30 Volts, 1350:1.35 Volts, 1400:1.40 Volts, 1450:1.45 Volts, 1500:1.50 Volts, 1550:1.55 Volts, 1600:1.60 Volts, 1650:1.65 Volts

Definition at line 288 of file FspmUpd.h.

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#### 8.4.2.87 UINT8 FSP\_M\_CONFIG::VmxEnable

Offset 0x02DA - Enable or Disable VMX Enable or Disable VMX; 0: Disable; 1: **Enable**.

\$EN\_DIS

Definition at line 824 of file FspmUpd.h.

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)

## 8.5 FSP\_M\_TEST\_CONFIG Struct Reference

Fsp M Test Configuration.

```
#include <FspmUpd.h>
```

### Public Attributes

- UINT32 [Signature](#)  
*Offset 0x0520.*
- UINT8 [SkipExtGfxScan](#)  
*Offset 0x0524 - Skip external display device scanning Enable: Do not scan for external display device, Disable (Default): Scan external display devices \$EN\_DIS.*
- UINT8 [BdatEnable](#)  
*Offset 0x0525 - Generate BIOS Data ACPI Table Enable: Generate BDAT for MRC RMT or SA PCIe data.*
- UINT8 [ScanExtGfxForLegacyOpRom](#)  
*Offset 0x0526 - Detect External Graphics device for LegacyOpROM Detect and report if external graphics device only support LegacyOpROM or not (to support CSM auto-enable).*
- UINT8 [LockPTMregs](#)  
*Offset 0x0527 - Lock PCU Thermal Management registers Lock PCU Thermal Management registers.*
- UINT8 [DmiVc1](#)  
*Offset 0x0528 - Enable/Disable DmiVc1 Enable/Disable DmiVc1.*
- UINT8 [DmiVcm](#)  
*Offset 0x0529 - Enable/Disable DmiVcm Enable/Disable DmiVcm.*
- UINT8 [DmiMaxLinkSpeed](#)  
*Offset 0x052A - DMI Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.*
- UINT8 [DmiGen3EqPh2Enable](#)  
*Offset 0x052B - DMI Equalization Phase 2 DMI Equalization Phase 2.*
- UINT8 [DmiGen3EqPh3Method](#)  
*Offset 0x052C - DMI Gen3 Equalization Phase3 DMI Gen3 Equalization Phase3.*
- UINT8 [Peg0Gen3EqPh2Enable](#)  
*Offset 0x052D - Phase2 EQ enable on the PEG 0:1:0.*
- UINT8 [Peg1Gen3EqPh2Enable](#)  
*Offset 0x052E - Phase2 EQ enable on the PEG 0:1:1.*
- UINT8 [Peg2Gen3EqPh2Enable](#)  
*Offset 0x052F - Phase2 EQ enable on the PEG 0:1:2.*
- UINT8 [Peg0Gen3EqPh3Method](#)  
*Offset 0x0530 - Phase3 EQ method on the PEG 0:1:0.*
- UINT8 [Peg1Gen3EqPh3Method](#)  
*Offset 0x0531 - Phase3 EQ method on the PEG 0:1:1.*



- UINT8 [Peg2Gen3EqPh3Method](#)  
*Offset 0x0532 - Phase3 EQ method on the PEG 0:1:2.*
  - UINT8 [PegGen3ProgramStaticEq](#)  
*Offset 0x0533 - Enable/Disable PEG GEN3 Static EQ Phase1 programming Program PEG Gen3 EQ Phase1 Static Presets.*
  - UINT8 [Gen3SwEqAlwaysAttempt](#)  
*Offset 0x0534 - PEG Gen3 SwEq Always Attempt Gen3 Software Equalization will be executed every boot.*
  - UINT8 [Gen3SwEqNumberOfPresets](#)  
*Offset 0x0535 - Select number of TxEq presets to test in the PCIe/DMI SwEq Select number of TxEq presets to test in the PCIe/DMI SwEq.*
  - UINT8 [Gen3SwEqEnableVocTest](#)  
*Offset 0x0536 - Enable use of the Voltage Offset and Centering Test in the PCIe SwEq Enable use of the Voltage Offset and Centering Test in the PCIe Software Equalization Algorithm.*
  - UINT8 [PegRxCemTestingMode](#)  
*Offset 0x0537 - PCIe Rx Compliance Testing Mode Disabled(0x0)(Default): Normal Operation - Disable PCIe Rx Compliance testing, Enabled(0x1): PCIe Rx Compliance Test Mode - PEG controller is in Rx Compliance Testing Mode; it should only be set when doing PCIe compliance testing \$EN\_DIS.*
  - UINT8 [PegRxCemLoopbackLane](#)  
*Offset 0x0538 - PCIe Rx Compliance Loopback Lane When PegRxCemTestingMode is Enabled the specified Lane (0 - 15) will be used for RxCEMLoopback.*
  - UINT8 [PegGenerateBdatMarginTable](#)  
*Offset 0x0539 - Generate PCIe BDAT Margin Table Set this policy to enable the generation and addition of PCIe margin data to the BDAT table.*
  - UINT8 [UnusedUpdSpace9](#) [6]  
*Offset 0x053A.*
  - UINT8 [PegRxCemNonProtocolAwareness](#)  
*Offset 0x0540 - PCIe Non-Protocol Awareness for Rx Compliance Testing Set this policy to enable the generation and addition of PCIe margin data to the BDAT table.*
  - UINT8 [PegGen3RxCtleOverride](#)  
*Offset 0x0541 - PCIe Override RxCTLE Disable(0x0)(Default): Normal Operation - RxCTLE adaptive behavior enabled, Enable(0x1): Override RxCTLE - Disable RxCTLE adaptive behavior to keep the configured RxCTLE peak values unmodified \$EN\_DIS.*
  - UINT8 [PegGen3Rsrd](#)  
*Offset 0x0542 - Rsrd Disable(0x0)(Default): Normal Operation - RxCTLE adaptive behavior enabled, Enable(0x1): Override RxCTLE - Disable RxCTLE adaptive behavior to keep the configured RxCTLE peak values unmodified \$EN\_DIS.*
  - UINT8 [PanelPowerEnable](#)  
*Offset 0x0543 - Panel Power Enable Control for enabling/disabling VDD force bit (Required only for early enabling of eDP panel).*
  - UINT8 [PegGen3RootPortPreset](#) [16]  
*Offset 0x0544 - PEG Gen3 Root port preset values per lane Used for programming PEG Gen3 preset values per lane.*
  - UINT8 [PegGen3EndPointPreset](#) [16]  
*Offset 0x0554 - PEG Gen3 End port preset values per lane Used for programming PEG Gen3 preset values per lane.*
  - UINT8 [PegGen3EndPointHint](#) [16]  
*Offset 0x0564 - PEG Gen3 End port Hint values per lane Used for programming PEG Gen3 Hint values per lane.*
  - UINT16 [Gen3SwEqJitterDwellTime](#)  
*Offset 0x0574 - Jitter Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 1000.*
  - UINT16 [Gen3SwEqJitterErrorTarget](#)  
*Offset 0x0576 - Jitter Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 1.*
  - UINT16 [Gen3SwEqVocDwellTime](#)  
*Offset 0x0578 - VOC Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 10000.*
  - UINT16 [Gen3SwEqVocErrorTarget](#)
-

- Offset 0x057A - VOC Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 2.
- UINT8 [SaPreMemTestRsvd](#) [4]  
Offset 0x057C - SaPreMemTestRsvd Reserved for SA Pre-Mem Test \$EN\_DIS.
  - UINT64 [BiosAcmBase](#)  
Offset 0x0580 - BiosAcmBase Enable/Disable.
  - UINT32 [BiosAcmSize](#)  
Offset 0x0588 - BiosAcmSize Enable/Disable.
  - UINT32 [TgaSize](#)  
Offset 0x058C - TgaSize Enable/Disable.
  - UINT64 [TxtLcpPdBase](#)  
Offset 0x0590 - TxtLcpPdBase Enable/Disable.
  - UINT64 [TxtLcpPdSize](#)  
Offset 0x0598 - TxtLcpPdSize Enable/Disable.
  - UINT16 [TotalFlashSize](#)  
Offset 0x05A0 - TotalFlashSize Enable/Disable.
  - UINT16 [BiosSize](#)  
Offset 0x05A2 - BiosSize Enable/Disable.
  - UINT8 [PchDciEn](#)  
Offset 0x05A4 - PCH Dci Enable Enable/disable PCH Dci.
  - UINT8 [PchDciAutoDetect](#)  
Offset 0x05A5 - PCH Dci Auto Detect Deprecated \$EN\_DIS.
  - UINT8 [SmbusDynamicPowerGating](#)  
Offset 0x05A6 - Smbus dynamic power gating Disable or Enable Smbus dynamic power gating.
  - UINT8 [WdtDisableAndLock](#)  
Offset 0x05A7 - Disable and Lock Watch Dog Register Set 1 to clear WDT status, then disable and lock WDT registers.
  - UINT8 [SmbusSpdWriteDisable](#)  
Offset 0x05A8 - SMBUS SPD Write Disable Set/Clear Smbus SPD Write Disable.
  - UINT8 [ChipsetInitMessage](#)  
Offset 0x05A9 - ChipsetInit HECI message Enable/Disable.
  - UINT8 [BypassPhySyncReset](#)  
Offset 0x05AA - Bypass ChipsetInit sync reset.
  - UINT8 [DidInitStat](#)  
Offset 0x05AB - Force ME DID Init Status Test, 0: disable, 1: Success, 2: No Memory in Channels, 3: Memory Init Error, 4: Memory not preserved across reset, Set ME DID init stat value \$EN\_DIS.
  - UINT8 [DisableCpuReplacedPolling](#)  
Offset 0x05AC - CPU Replaced Polling Disable Test, 0: disable, 1: enable, Setting this option disables CPU replacement polling loop \$EN\_DIS.
  - UINT8 [SendDidMsg](#)  
Offset 0x05AD - ME DID Message Test, 0: disable, 1: enable, Enable/Disable ME DID Message (disable will prevent the DID message from being sent) \$EN\_DIS.
  - UINT8 [DisableHeciRetry](#)  
Offset 0x05AE - Retry mechanism for HECI APIs Test, 0: disable, 1: enable, Enable/Disable HECI retry.
  - UINT8 [DisableMessageCheck](#)  
Offset 0x05AF - Check HECI message before send Test, 0: disable, 1: enable, Enable/Disable message check.
  - UINT8 [SkipMbpHob](#)  
Offset 0x05B0 - Skip MBP HOB Test, 0: disable, 1: enable, Enable/Disable MOB HOB.
  - UINT8 [HeciCommunication2](#)  
Offset 0x05B1 - HECI2 Interface Communication Test, 0: disable, 1: enable, Adds or Removes HECI2 Device from PCI space.
  - UINT8 [KtDeviceEnable](#)  
Offset 0x05B2 - Enable KT device Test, 0: disable, 1: enable, Enable or Disable KT device.
-

- UINT8 [IderDeviceEnable](#)  
*Offset 0x05B3 - Enable IDeR Test, 0: disable, 1: enable, Enable or Disable IDeR.*
- UINT8 [ReservedFspmTestUpd](#) [12]  
*Offset 0x05B4.*

### 8.5.1 Detailed Description

Fsp M Test Configuration.

Definition at line 1301 of file FspmUpd.h.

### 8.5.2 Member Data Documentation

#### 8.5.2.1 UINT8 FSP\_M\_TEST\_CONFIG::BdatEnable

Offset 0x0525 - Generate BIOS Data ACPI Table Enable: Generate BDAT for MRC RMT or SA PCIe data.

Disable (Default): Do not generate it \$EN\_DIS

Definition at line 1318 of file FspmUpd.h.

#### 8.5.2.2 UINT64 FSP\_M\_TEST\_CONFIG::BiosAcmbase

Offset 0x0580 - BiosAcmbase Enable/Disable.

0: Disable, define default value of BiosAcmbase , 1: enable

Definition at line 1554 of file FspmUpd.h.

#### 8.5.2.3 UINT32 FSP\_M\_TEST\_CONFIG::BiosAcmsize

Offset 0x0588 - BiosAcmsize Enable/Disable.

0: Disable, define default value of BiosAcmsize , 1: enable

Definition at line 1559 of file FspmUpd.h.

#### 8.5.2.4 UINT16 FSP\_M\_TEST\_CONFIG::BiosSize

Offset 0x05A2 - BiosSize Enable/Disable.

0: Disable, define default value of BiosSize , 1: enable

Definition at line 1584 of file FspmUpd.h.

#### 8.5.2.5 UINT8 FSP\_M\_TEST\_CONFIG::BypassPhySyncReset

Offset 0x05AA - Bypass ChipsetInit sync reset.

0: disable, 1: enable, Set Enable to bypass the reset after ChipsetInit HECI message. \$EN\_DIS

Definition at line 1628 of file FspmUpd.h.

#### 8.5.2.6 UINT8 FSP\_M\_TEST\_CONFIG::ChipsetInitMessage

Offset 0x05A9 - ChipsetInit HECI message Enable/Disable.

0: Disable, 1: enable, Enable or disable ChipsetInit HECI message. If disabled, it prevents from sending ChipsetInit HECI message. \$EN\_DIS

Definition at line 1622 of file FspmUpd.h.

#### 8.5.2.7 UINT8 FSP\_M\_TEST\_CONFIG::DisableHeciRetry

Offset 0x05AE - Retry mechanism for HECI APIs Test, 0: disable, 1: enable, Enable/Disable HECI retry.

\$EN\_DIS

Definition at line 1654 of file FspmUpd.h.

#### 8.5.2.8 UINT8 FSP\_M\_TEST\_CONFIG::DisableMessageCheck

Offset 0x05AF - Check HECI message before send Test, 0: disable, 1: enable, Enable/Disable message check.

\$EN\_DIS

Definition at line 1660 of file FspmUpd.h.

#### 8.5.2.9 UINT8 FSP\_M\_TEST\_CONFIG::DmiGen3EqPh2Enable

Offset 0x052B - DMI Equalization Phase 2 DMI Equalization Phase 2.

(0x0): Disable phase 2, (0x1): Enable phase 2, (0x2)(Default): AUTO - Use the current default method 0:Disable phase2, 1:Enable phase2, 2:Auto

Definition at line 1357 of file FspmUpd.h.

#### 8.5.2.10 UINT8 FSP\_M\_TEST\_CONFIG::DmiGen3EqPh3Method

Offset 0x052C - DMI Gen3 Equalization Phase3 DMI Gen3 Equalization Phase3.

Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line 1367 of file FspmUpd.h.

#### 8.5.2.11 UINT8 FSP\_M\_TEST\_CONFIG::DmiVc1

Offset 0x0528 - Enable/Disable DmiVc1 Enable/Disable DmiVc1.

Enable = 1, Disable (Default) = 0 \$EN\_DIS

Definition at line 1337 of file FspmUpd.h.

#### 8.5.2.12 UINT8 FSP\_M\_TEST\_CONFIG::DmiVcm

Offset 0x0529 - Enable/Disable DmiVcm Enable/Disable DmiVcm.

Enable (Default) = 1, Disable = 0 \$EN\_DIS

Definition at line 1343 of file FspmUpd.h.

#### 8.5.2.13 UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqAlwaysAttempt

Offset 0x0534 - PEG Gen3 SwEq Always Attempt Gen3 Software Equalization will be executed every boot.

Disabled(0x0)(Default): Reuse EQ settings saved/restored from NVRAM whenever possible, Enabled(0x1): Re-test and generate new EQ values every boot, not recommended 0:Disable, 1:Enable

Definition at line 1433 of file FspmUpd.h.

#### 8.5.2.14 UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqEnableVocTest

Offset 0x0536 - Enable use of the Voltage Offset and Centering Test in the PCIe SwEq Enable use of the Voltage Offset and Centering Test in the PCIe Software Equalization Algorithm.

Disabled(0x0): Disable VOC Test, Enabled(0x1): Enable VOC Test, Auto(0x2)(Default): Use the current default 0:Disable, 1:Enable, 2:Auto

Definition at line 1451 of file FspmUpd.h.

#### 8.5.2.15 UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqJitterDwellTime

Offset 0x0574 - Jitter Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 1000.

##### Warning

Do not change from the default

Definition at line 1528 of file FspmUpd.h.

#### 8.5.2.16 UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqJitterErrorTarget

Offset 0x0576 - Jitter Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 1.

##### Warning

Do not change from the default

Definition at line 1533 of file FspmUpd.h.

#### 8.5.2.17 UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqNumberOfPresets

Offset 0x0535 - Select number of TxEq presets to test in the PCIe/DMI SwEq Select number of TxEq presets to test in the PCIe/DMI SwEq.

P7,P3,P5(0x0): Test Presets 7, 3, and 5, P0-P9(0x1): Test Presets 0-9, Auto(0x2)(Default): Use the current default method (Default)Auto will test Presets 7, 3, and 5. It is possible for this default to change over time;using Auto will ensure Reference Code always uses the latest default settings 0:P7 P3 P5, 1:P0 to P9, 2:Auto

Definition at line 1443 of file FspmUpd.h.

#### 8.5.2.18 UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqVocDwellTime

Offset 0x0578 - VOC Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 10000.

##### Warning

Do not change from the default

Definition at line 1538 of file FspmUpd.h.

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**8.5.2.19 UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqVocErrorTarget**

Offset 0x057A - VOC Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 2.

**Warning**

Do not change from the default

Definition at line 1543 of file FspmUpd.h.

**8.5.2.20 UINT8 FSP\_M\_TEST\_CONFIG::HeciCommunication2**

Offset 0x05B1 - HECI2 Interface Communication Test, 0: disable, 1: enable, Adds or Removes HECI2 Device from PCI space.

\$EN\_DIS

Definition at line 1672 of file FspmUpd.h.

**8.5.2.21 UINT8 FSP\_M\_TEST\_CONFIG::IdlerDeviceEnable**

Offset 0x05B3 - Enable IDer Test, 0: disable, 1: enable, Enable or Disable IDer.

\$EN\_DIS

Definition at line 1684 of file FspmUpd.h.

**8.5.2.22 UINT8 FSP\_M\_TEST\_CONFIG::KtDeviceEnable**

Offset 0x05B2 - Enable KT device Test, 0: disable, 1: enable, Enable or Disable KT device.

\$EN\_DIS

Definition at line 1678 of file FspmUpd.h.

**8.5.2.23 UINT8 FSP\_M\_TEST\_CONFIG::LockPTMregs**

Offset 0x0527 - Lock PCU Thermal Management registers Lock PCU Thermal Management registers.

Enable(Default)=1, Disable=0 \$EN\_DIS

Definition at line 1331 of file FspmUpd.h.

**8.5.2.24 UINT8 FSP\_M\_TEST\_CONFIG::PanelPowerEnable**

Offset 0x0543 - Panel Power Enable Control for enabling/disabling VDD force bit (Required only for early enabling of eDP panel).

0=Disable, 1(Default)=Enable \$EN\_DIS

Definition at line 1508 of file FspmUpd.h.

**8.5.2.25 UINT8 FSP\_M\_TEST\_CONFIG::PchDciEn**

Offset 0x05A4 - PCH Dci Enable Enable/disable PCH Dci.

\$EN\_DIS

Definition at line 1590 of file FspmUpd.h.

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**8.5.2.26 UINT8 FSP\_M\_TEST\_CONFIG::Peg0Gen3EqPh2Enable**

Offset 0x052D - Phase2 EQ enable on the PEG 0:1:0.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line 1374 of file FspmUpd.h.

**8.5.2.27 UINT8 FSP\_M\_TEST\_CONFIG::Peg0Gen3EqPh3Method**

Offset 0x0530 - Phase3 EQ method on the PEG 0:1:0.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line 1398 of file FspmUpd.h.

**8.5.2.28 UINT8 FSP\_M\_TEST\_CONFIG::Peg1Gen3EqPh2Enable**

Offset 0x052E - Phase2 EQ enable on the PEG 0:1:1.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line 1381 of file FspmUpd.h.

**8.5.2.29 UINT8 FSP\_M\_TEST\_CONFIG::Peg1Gen3EqPh3Method**

Offset 0x0531 - Phase3 EQ method on the PEG 0:1:1.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line 1408 of file FspmUpd.h.

**8.5.2.30 UINT8 FSP\_M\_TEST\_CONFIG::Peg2Gen3EqPh2Enable**

Offset 0x052F - Phase2 EQ enable on the PEG 0:1:2.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line 1388 of file FspmUpd.h.

**8.5.2.31 UINT8 FSP\_M\_TEST\_CONFIG::Peg2Gen3EqPh3Method**

Offset 0x0532 - Phase3 EQ method on the PEG 0:1:2.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line 1418 of file FspmUpd.h.

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**8.5.2.32    UINT8 FSP\_M\_TEST\_CONFIG::PegGen3EndPointHint[16]**

Offset 0x0564 - PEG Gen3 End port Hint values per lane Used for programming PEG Gen3 Hint values per lane.

Range: 0-6, 2 is default for each lane

Definition at line 1523 of file FspmUpd.h.

**8.5.2.33    UINT8 FSP\_M\_TEST\_CONFIG::PegGen3EndPointPreset[16]**

Offset 0x0554 - PEG Gen3 End port preset values per lane Used for programming PEG Gen3 preset values per lane.

Range: 0-9, 7 is default for each lane

Definition at line 1518 of file FspmUpd.h.

**8.5.2.34    UINT8 FSP\_M\_TEST\_CONFIG::PegGen3ProgramStaticEq**

Offset 0x0533 - Enable/Disable PEG GEN3 Static EQ Phase1 programming Program PEG Gen3 EQ Phase1 Static Presets.

Disabled(0x0): Disable EQ Phase1 Static Presets Programming, Enabled(0x1)(Default): Enable EQ Phase1 Static Presets Programming \$EN\_DIS

Definition at line 1425 of file FspmUpd.h.

**8.5.2.35    UINT8 FSP\_M\_TEST\_CONFIG::PegGen3RootPortPreset[16]**

Offset 0x0544 - PEG Gen3 Root port preset values per lane Used for programming PEG Gen3 preset values per lane.

Range: 0-9, 8 is default for each lane

Definition at line 1513 of file FspmUpd.h.

**8.5.2.36    UINT8 FSP\_M\_TEST\_CONFIG::PegGenerateBdatMarginTable**

Offset 0x0539 - Generate PCIe BDAT Margin Table Set this policy to enable the generation and addition of PCIe margin data to the BDAT table.

Disabled(0x0)(Default): Normal Operation - Disable PCIe BDAT margin data generation, Enable(0x1): Generate PCIe BDAT margin data \$EN\_DIS

Definition at line 1472 of file FspmUpd.h.

**8.5.2.37    UINT8 FSP\_M\_TEST\_CONFIG::PegRxCemLoopbackLane**

Offset 0x0538 - PCIe Rx Compliance Loopback Lane When PegRxCemTestingMode is Enabled the specified Lane (0 - 15) will be used for RxCEMLoopback.

Default is Lane 0

Definition at line 1464 of file FspmUpd.h.

**8.5.2.38    UINT8 FSP\_M\_TEST\_CONFIG::PegRxCemNonProtocolAwareness**

Offset 0x0540 - PCIe Non-Protocol Awareness for Rx Compliance Testing Set this policy to enable the generation and addition of PCIe margin data to the BDAT table.

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Disabled(0x0)(Default): Normal Operation - Disable non-protocol awareness, Enable(0x1): Non-Protocol Awareness Enabled - Enable non-protocol awareness for compliance testing \$EN\_DIS

Definition at line 1485 of file FspmUpd.h.

#### 8.5.2.39 UINT8 FSP\_M\_TEST\_CONFIG::ScanExtGfxForLegacyOpRom

Offset 0x0526 - Detect External Graphics device for LegacyOpROM Detect and report if external graphics device only support LegacyOpROM or not (to support CSM auto-enable).

Enable(Default)=1, Disable=0 \$EN\_DIS

Definition at line 1325 of file FspmUpd.h.

#### 8.5.2.40 UINT8 FSP\_M\_TEST\_CONFIG::SkipMbpHob

Offset 0x05B0 - Skip MBP HOB Test, 0: disable, 1: enable, Enable/Disable MOB HOB.

\$EN\_DIS

Definition at line 1666 of file FspmUpd.h.

#### 8.5.2.41 UINT8 FSP\_M\_TEST\_CONFIG::SmbusDynamicPowerGating

Offset 0x05A6 - Smbus dynamic power gating Disable or Enable Smbus dynamic power gating.

\$EN\_DIS

Definition at line 1602 of file FspmUpd.h.

#### 8.5.2.42 UINT8 FSP\_M\_TEST\_CONFIG::SmbusSpdWriteDisable

Offset 0x05A8 - SMBUS SPD Write Disable Set/Clear Smbus SPD Write Disable.

0: leave SPD Write Disable bit; 1: set SPD Write Disable bit. For security recommendations, SPD write disable bit must be set. \$EN\_DIS

Definition at line 1615 of file FspmUpd.h.

#### 8.5.2.43 UINT32 FSP\_M\_TEST\_CONFIG::TgaSize

Offset 0x058C - TgaSize Enable/Disable.

0: Disable, define default value of TgaSize , 1: enable

Definition at line 1564 of file FspmUpd.h.

#### 8.5.2.44 UINT16 FSP\_M\_TEST\_CONFIG::TotalFlashSize

Offset 0x05A0 - TotalFlashSize Enable/Disable.

0: Disable, define default value of TotalFlashSize , 1: enable

Definition at line 1579 of file FspmUpd.h.

#### 8.5.2.45 UINT64 FSP\_M\_TEST\_CONFIG::TxtLcpPdBase

Offset 0x0590 - TxtLcpPdBase Enable/Disable.

0: Disable, define default value of TxtLcpPdBase , 1: enable

---

Definition at line 1569 of file FspmUpd.h.

#### 8.5.2.46 UINT64 FSP\_M\_TEST\_CONFIG::TxtLcpPdSize

Offset 0x0598 - TxtLcpPdSize Enable/Disable.

0: Disable, define default value of TxtLcpPdSize , 1: enable

Definition at line 1574 of file FspmUpd.h.

#### 8.5.2.47 UINT8 FSP\_M\_TEST\_CONFIG::WdtDisableAndLock

Offset 0x05A7 - Disable and Lock Watch Dog Register Set 1 to clear WDT status, then disable and lock WDT registers.

\$EN\_DIS

Definition at line 1608 of file FspmUpd.h.

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)

## 8.6 FSP\_S\_CONFIG Struct Reference

Fsp S Configuration.

```
#include <FspsUpd.h>
```

### Public Attributes

- UINT32 [LogoPtr](#)  
*Offset 0x0020 - Logo Pointer Points to PEI Display Logo Image.*
- UINT32 [LogoSize](#)  
*Offset 0x0024 - Logo Size Size of PEI Display Logo Image.*
- UINT32 [GraphicsConfigPtr](#)  
*Offset 0x0028 - Graphics Configuration Ptr Points to VBT.*
- UINT8 [Device4Enable](#)  
*Offset 0x002C - Enable Device 4 Enable/disable Device 4 \$EN\_DIS.*
- UINT8 [PchHdaEnable](#)  
*Offset 0x002D - Enable Intel HD Audio (Azalia) Enable/disable Azalia controller.*
- UINT8 [PchHdaDspEnable](#)  
*Offset 0x002E - Enable HD Audio DSP Enable/disable HD Audio DSP feature.*
- UINT8 [PchHdaIoBufferOwnership](#)  
*Offset 0x002F - Select HDAudio IoBuffer Ownership Indicates the ownership of the I/O buffer between Intel HD Audio link vs I2S0 / I2S port.*
- UINT8 [PchCio2Enable](#)  
*Offset 0x0030 - Enable CIO2 Controller Enable/disable SKYCAM CIO2 Controller.*
- UINT8 [ScsEmmcEnabled](#)  
*Offset 0x0031 - Enable eMMC Controller Enable/disable eMMC Controller.*
- UINT8 [ScsEmmcHs400Enabled](#)  
*Offset 0x0032 - Enable eMMC HS400 Mode Enable eMMC HS400 Mode.*
- UINT8 [ScsSdCardEnabled](#)  
*Offset 0x0033 - Enable SdCard Controller Enable/disable SD Card Controller.*

- UINT8 [PchIshEnable](#)  
*Offset 0x0034 - Enable PCH ISH Controller Enable/disable ISH Controller.*
- UINT8 [ShowSpiController](#)  
*Offset 0x0035 - Show SPI controller Enable/disable to show SPI controller.*
- UINT8 [SpiFlashCfgLockDown](#)  
*Offset 0x0036 - Flash Configuration Lock Down Enable/disable flash lock down.*
- UINT8 [UnusedUpdSpace0](#)  
*Offset 0x0037.*
- UINT32 [MicrocodeRegionBase](#)  
*Offset 0x0038 - MicrocodeRegionBase Memory Base of Microcode Updates.*
- UINT32 [MicrocodeRegionSize](#)  
*Offset 0x003C - MicrocodeRegionSize Size of Microcode Updates.*
- UINT8 [TurboMode](#)  
*Offset 0x0040 - Turbo Mode Enable/Disable Turbo mode.*
- UINT8 [SataSalpSupport](#)  
*Offset 0x0041 - Enable SATA SALP Support Enable/disable SATA Aggressive Link Power Management.*
- UINT8 [SataPortsEnable](#) [8]  
*Offset 0x0042 - Enable SATA ports Enable/disable SATA ports.*
- UINT8 [SataPortsDevSlp](#) [8]  
*Offset 0x004A - Enable SATA DEVSLP Feature Enable/disable SATA DEVSLP per port.*
- UINT8 [PortUsb20Enable](#) [16]  
*Offset 0x0052 - Enable USB2 ports Enable/disable per USB2 ports.*
- UINT8 [PortUsb30Enable](#) [10]  
*Offset 0x0062 - Enable USB3 ports Enable/disable per USB3 ports.*
- UINT8 [XdcIEnable](#)  
*Offset 0x006C - Enable xDCI controller Enable/disable to xDCI controller.*
- UINT8 [SsicPortEnable](#)  
*Offset 0x006D - Enable XHCI SSIC Enable Enable/disable XHCI SSIC port.*
- UINT8 [UnusedUpdSpace1](#)  
*Offset 0x006E.*
- UINT8 [NumOfDevIntConfig](#)  
*Offset 0x006F - Number of DevIntConfig Entry Number of Device Interrupt Configuration Entry.*
- UINT32 [DevIntConfigPtr](#)  
*Offset 0x0070 - Address of PCH\_DEVICE\_INTERRUPT\_CONFIG table.*
- UINT8 [SerialIoDevMode](#) [11]  
*Offset 0x0074 - Enable SerialIo Device Mode 0:Disabled, 1:ACPI Mode, 2:PCI Mode, 3:Hidden mode, 4:Legacy UA↔RT mode - Enable/disable SerialIo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5,SPI0,SPI1,UART0,UART1,UART2 device mode respectively.*
- UINT8 [PxRcConfig](#) [8]  
*Offset 0x007F - PIRQx to IRQx Map Config PIRQx to IRQx mapping.*
- UINT8 [GpioIrqRoute](#)  
*Offset 0x0087 - Select GPIO IRQ Route GPIO IRQ Select.*
- UINT8 [ScIrqSelect](#)  
*Offset 0x0088 - Select ScIrqSelect SCI IRQ Select.*
- UINT8 [TcoIrqSelect](#)  
*Offset 0x0089 - Select TcoIrqSelect TCO IRQ Select.*
- UINT8 [TcoIrqEnable](#)  
*Offset 0x008A - Enable/Disable Tco IRQ Enable/disable TCO IRQ \$EN\_DIS.*
- UINT8 [PchHdaVerbTableEntryNum](#)  
*Offset 0x008B - PCH HDA Verb Table Entry Number Number of Entries in Verb Table.*
- UINT32 [PchHdaVerbTablePtr](#)

- Offset 0x008C - PCH HDA Verb Table Pointer Pointer to Array of pointers to Verb Table.
  - UIN8 [UnusedUpdSpace2](#)
    - Offset 0x0090.
  - UIN8 [SataEnable](#)
    - Offset 0x0091 - Enable SATA Enable/disable SATA controller.
  - UIN8 [SataMode](#)
    - Offset 0x0092 - SATA Mode Select SATA controller working mode.
  - UIN8 [Usb2AfePetxiset](#) [16]
    - Offset 0x0093 - USB Per Port HS Preemphasis Bias USB Per Port HS Preemphasis Bias.
  - UIN8 [Usb2AfeTxiset](#) [16]
    - Offset 0x00A3 - USB Per Port HS Transmitter Bias USB Per Port HS Transmitter Bias.
  - UIN8 [Usb2AfePredeemp](#) [16]
    - Offset 0x00B3 - USB Per Port HS Transmitter Emphasis USB Per Port HS Transmitter Emphasis.
  - UIN8 [Usb2AfePehalfbit](#) [16]
    - Offset 0x00C3 - USB Per Port Half Bit Pre-emphasis USB Per Port Half Bit Pre-emphasis.
  - UIN8 [Usb3HsioTxDeEmphEnable](#) [10]
    - Offset 0x00D3 - Enable the write to USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Enable the write to USB 3.0 TX Output -3.5dB De-Emphasis Adjustment.
  - UIN8 [Usb3HsioTxDeEmph](#) [10]
    - Offset 0x00DD - USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Setting USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Setting, HSIO\_TX\_DWORD5[21:16], **Default = 29h** (approximately -3.5dB De-Emphasis).
  - UIN8 [Usb3HsioTxDownscaleAmpEnable](#) [10]
    - Offset 0x00E7 - Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment, Each value in array can be between 0-1.
  - UIN8 [Usb3HsioTxDownscaleAmp](#) [10]
    - Offset 0x00F1 - USB 3.0 TX Output Downscale Amplitude Adjustment USB 3.0 TX Output Downscale Amplitude Adjustment, HSIO\_TX\_DWORD8[21:16], **Default = 00h**.
  - UIN8 [PchLanEnable](#)
    - Offset 0x00FB - Enable LAN Enable/disable LAN controller.
  - UIN8 [DelayUsbPdoProgramming](#)
    - Offset 0x00FC - Delay USB PDO Programming Enable/disable delay of PDO programming for USB from PEI phase to DXE phase.
  - UIN8 [UnusedUpdSpace3](#) [23]
    - Offset 0x00FD.
  - UIN8 [PcieRpClkReqSupport](#) [24]
    - Offset 0x0114 - Enable PCIE RP CLKREQ Support Enable/disable PCIE Root Port CLKREQ support.
  - UIN8 [PcieRpClkReqNumber](#) [24]
    - Offset 0x012C - Configure CLKREQ Number Configure Root Port CLKREQ Number if CLKREQ is supported.
  - UIN8 [UnusedUpdSpace4](#) [5]
    - Offset 0x0144.
  - UIN8 [Heci3Enabled](#)
    - Offset 0x0149 - HECI3 state The HECI3 state from Mbp for reference in S3 path or when MbpHob is not installed.
  - UIN8 [UnusedUpdSpace5](#) [9]
    - Offset 0x014A.
  - UIN8 [AmtEnabled](#)
    - Offset 0x0153 - AMT Switch Enable/Disable.
  - UIN8 [WatchDog](#)
    - Offset 0x0154 - WatchDog Timer Switch Enable/Disable.
  - UIN8 [AsfEnabled](#)
    - Offset 0x0155 - ASF Switch Enable/Disable.
  - UIN8 [ManageabilityMode](#)
    - Offset 0x0156 - Manageability Mode set by Mebx Enable/Disable.
-

- UINT8 [FwProgress](#)  
*Offset 0x0157 - PET Progress Enable/Disable.*
- UINT16 [WatchDogTimerOs](#)  
*Offset 0x0158 - OS Timer 16 bits Value, Set OS watchdog timer.*
- UINT16 [WatchDogTimerBios](#)  
*Offset 0x015A - BIOS Timer 16 bits Value, Set BIOS watchdog timer.*
- UINT8 [AmtSolEnabled](#)  
*Offset 0x015C - SOL Switch Enable/Disable.*
- UINT8 [PcieRpClkSrcNumber](#) [24]  
*Offset 0x015D - Configure CLKSRC Number Configure Root Port CLKSRC Number.*
- UINT8 [PcieRpForceClkDisableWhenRpDisable](#) [24]  
*Offset 0x0175 - Force Disable clock Disables clock even if link is inactive default value is 0.*
- UINT8 [UnusedUpdSpace6](#) [115]  
*Offset 0x018D.*
- UINT16 [DefaultSvid](#)  
*Offset 0x0200 - Subsystem Vendor ID for SA devices Subsystem ID that will be programmed to SA devices: Default SubSystemVendorId=0x8086.*
- UINT16 [DefaultSid](#)  
*Offset 0x0202 - Subsystem Device ID for SA devices Subsystem ID that will be programmed to SA devices: Default SubSystemId=0x2015.*
- UINT8 [CridEnable](#)  
*Offset 0x0204 - Enable/Disable SA CRID Enable: SA CRID, Disable (Default): SA CRID \$EN\_DIS.*
- UINT8 [DmiAspm](#)  
*Offset 0x0205 - DMI ASPM 0=Disable, 2(Default)=L1 0:Disable, 2:L1.*
- UINT16 [PegPhysicalSlotNumber](#) [3]  
*Offset 0x0206 - PCIe Physical Slot Number per root port Physical Slot Number per root port.*
- UINT8 [PegDeEmphasis](#) [3]  
*Offset 0x020C - PCIe DeEmphasis control per root port 0: -6dB, 1(Default): -3.5dB 0:-6dB, 1:-3.5dB.*
- UINT8 [PegSlotPowerLimitValue](#) [3]  
*Offset 0x020F - PCIe Slot Power Limit value per root port Slot power limit value per root port.*
- UINT8 [PegSlotPowerLimitScale](#) [3]  
*Offset 0x0212 - PCIe Slot Power Limit scale per root port Slot power limit scale per root port 0:1.0x, 1:0.1x, 2:0.01x, 3:0x001x.*
- UINT8 [PavpEnable](#)  
*Offset 0x0215 - Enable/Disable PavpEnable Enable(Default): Enable PavpEnable, Disable: Disable PavpEnable \$EN\_DIS.*
- UINT8 [CdClock](#)  
*Offset 0x0216 - CdClock Frequency selection 0=337.5 Mhz, 1=450 Mhz, 2=540 Mhz, 3(Default)= 675 Mhz 0: 337.5 Mhz, 1: 450 Mhz, 2: 540 Mhz, 3: 675 Mhz.*
- UINT8 [PeiGraphicsPeimInit](#)  
*Offset 0x0217 - Enable/Disable PeiGraphicsPeimInit Enable: Enable PeiGraphicsPeimInit, Disable(Default): Disable PeiGraphicsPeimInit \$EN\_DIS.*
- UINT8 [SalmguEnable](#)  
*Offset 0x0218 - Enable/Disable SA IMGU(SKYCAME) Enable(Default): Enable SA IMGU(SKYCAME), Disable: Disable SA IMGU(SKYCAME) \$EN\_DIS.*
- UINT8 [GmmEnable](#)  
*Offset 0x0219 - Enable or disable GMM device 0=Disable, 1(Default)=Enable \$EN\_DIS.*
- UINT8 [X2ApicOptOut](#)  
*Offset 0x021A - State of X2APIC\_OPT\_OUT bit in the DMAR table 0=Disable/Clear, 1=Enable/Set \$EN\_DIS.*
- UINT8 [UnusedUpdSpace7](#) [1]  
*Offset 0x021B.*
- UINT32 [VtdBaseAddress](#) [2]

Offset 0x021C - Base addresses for VT-d function MMIO access Base addresses for VT-d MMIO access per VT-d engine.

- UINT8 [ProgramGtChickenBits](#)

Offset 0x0224 - Program GT Chicken bits Program the GT chicken bits in GTTMMADR + 0xD00 BITS [3:1].

- UINT8 [UnusedUpdSpace8](#) [18]

Offset 0x0225.

- UINT8 [SaPostMemProductionRsvd](#) [15]

Offset 0x0237 - SaPostMemProductionRsvd Reserved for SA Post-Mem Production \$EN\_DIS.

- UINT8 [UnusedUpdSpace9](#) [8]

Offset 0x0246.

- UINT8 [Psi3Enable](#) [5]

Offset 0x024E - Power State 3 enable/disable PCODE MMIO Mailbox: Power State 3 enable/disable; 0: Disable; 1: **Enable**.

- UINT8 [Psi4Enable](#) [5]

Offset 0x0253 - Power State 4 enable/disable PCODE MMIO Mailbox: Power State 4 enable/disable; 0: Disable; 1: **Enable**. For all VR Indexes.

- UINT8 [ImonSlope](#) [5]

Offset 0x0258 - Imon slope correction PCODE MMIO Mailbox: Imon slope correction.

- UINT8 [ImonOffset](#) [5]

Offset 0x025D - Imon offset correction PCODE MMIO Mailbox: Imon offset correction.

- UINT8 [VrConfigEnable](#) [5]

Offset 0x0262 - Enable/Disable BIOS configuration of VR Enable/Disable BIOS configuration of VR; 0: **Disable**; 1: **Enable**. For all VR Indexes.

- UINT8 [TdcEnable](#) [5]

Offset 0x0267 - Thermal Design Current enable/disable PCODE MMIO Mailbox: Thermal Design Current enable/disable; 0: **Disable**; 1: **Enable**. For all VR Indexes.

- UINT8 [TdcTimeWindow](#) [5]

Offset 0x026C - HECI3 state PCODE MMIO Mailbox: Thermal Design Current time window.

- UINT8 [TdcLock](#) [5]

Offset 0x0271 - Thermal Design Current Lock PCODE MMIO Mailbox: Thermal Design Current Lock; 0: **Disable**; 1: **Enable**. For all VR Indexes.

- UINT8 [PsysSlope](#)

Offset 0x0276 - Platform Psys slope correction PCODE MMIO Mailbox: Platform Psys slope correction.

- UINT8 [PsysOffset](#)

Offset 0x0277 - Platform Psys offset correction PCODE MMIO Mailbox: Platform Psys offset correction.

- UINT8 [AcousticNoiseMitigation](#)

Offset 0x0278 - Acoustic Noise Mitigation feature Enable or Disable Acoustic Noise Mitigation feature.

- UINT8 [FastPkgCRampDisablela](#)

Offset 0x0279 - Disable Fast Slew Rate for Deep Package C States for VR IA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

- UINT8 [SlowSlewRateForla](#)

Offset 0x027A - Slew Rate configuration for Deep Package C States for VR IA domain Slew Rate configuration for Deep Package C States for VR IA domain based on Acoustic Noise Mitigation feature enabled.

- UINT8 [SlowSlewRateForGt](#)

Offset 0x027B - Slew Rate configuration for Deep Package C States for VR GT domain Slew Rate configuration for Deep Package C States for VR GT domain based on Acoustic Noise Mitigation feature enabled.

- UINT8 [SlowSlewRateForSa](#)

Offset 0x027C - Slew Rate configuration for Deep Package C States for VR SA domain Slew Rate configuration for Deep Package C States for VR SA domain based on Acoustic Noise Mitigation feature enabled.

- UINT8 [UnusedUpdSpace10](#) [9]

Offset 0x027D.

- UINT16 [TdcPowerLimit](#) [5]

Offset 0x0286 - Thermal Design Current current limit PCODE MMIO Mailbox: Thermal Design Current current limit.

- UINT32 [VrPowerDeliveryDesign](#)  
*Offset 0x0290 - CPU VR Power Delivery Design Used to communicate the power delivery design capability of the board.*
  - UINT8 [UnusedUpdSpace11](#) [4]  
*Offset 0x0294.*
  - UINT16 [AcLoadline](#) [5]  
*Offset 0x0298 - AcLoadline PCODE MMIO Mailbox: AcLoadline in 1/100 mOhms (ie.*
  - UINT16 [DcLoadline](#) [5]  
*Offset 0x02A2 - DcLoadline PCODE MMIO Mailbox: DcLoadline in 1/100 mOhms (ie.*
  - UINT16 [Psi1Threshold](#) [5]  
*Offset 0x02AC - Power State 1 Threshold current PCODE MMIO Mailbox: Power State 1 current cutoff in 1/4 Amp increments.*
  - UINT16 [Psi2Threshold](#) [5]  
*Offset 0x02B6 - Power State 2 Threshold current PCODE MMIO Mailbox: Power State 2 current cutoff in 1/4 Amp increments.*
  - UINT16 [Psi3Threshold](#) [5]  
*Offset 0x02C0 - Power State 3 Threshold current PCODE MMIO Mailbox: Power State 3 current cutoff in 1/4 Amp increments.*
  - UINT16 [IccMax](#) [5]  
*Offset 0x02CA - Icc Max limit PCODE MMIO Mailbox: VR Icc Max limit.*
  - UINT16 [VrVoltageLimit](#) [5]  
*Offset 0x02D4 - VR Voltage Limit PCODE MMIO Mailbox: VR Voltage Limit.*
  - UINT8 [UnusedUpdSpace12](#)  
*Offset 0x02DE.*
  - UINT8 [FastPkgCRampDisableGt](#)  
*Offset 0x02DF - Disable Fast Slew Rate for Deep Package C States for VR GT domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.*
  - UINT8 [FastPkgCRampDisableSa](#)  
*Offset 0x02E0 - Disable Fast Slew Rate for Deep Package C States for VR SA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.*
  - UINT8 [UnusedUpdSpace13](#)  
*Offset 0x02E1.*
  - UINT8 [SendVrMbxCmd](#)  
*Offset 0x02E2 - Enable VR specific mailbox command VR specific mailbox commands.*
  - UINT8 [SendVrMbxCmd1](#)  
*Offset 0x02E3 - Select VR specific mailbox command to send VR specific mailbox commands.*
  - UINT32 [CpuS3ResumeMtrrData](#)  
*Offset 0x02E4 - CpuS3ResumeMtrrData Pointer to CPU S3 Resume MTRR Data.*
  - CPU\_CONFIG\_FSP\_DATA [CpuConfig](#)  
*Offset 0x02E8 - Cpu Configuration Cpu Configuration data.*
  - UINT64 [MicrocodePatchAddress](#)  
*Offset 0x02F0 - MicrocodePatchAddress Pointer to microcode patch that is suitable for this processor.*
  - UINT16 [CpuS3ResumeMtrrDataSize](#)  
*Offset 0x02F8 - CpuS3ResumeMtrrDataSize Size of S3 resume MTRR data.*
  - UINT8 [UnusedUpdSpace14](#)  
*Offset 0x02FA.*
  - UINT8 [PchSkyCamPortATermOvrEnable](#)  
*Offset 0x02FB - Enable SkyCam PortA Termination override Enable/disable PortA Termination override.*
  - UINT8 [PchSkyCamPortBTermOvrEnable](#)  
*Offset 0x02FC - Enable SkyCam PortB Termination override Enable/disable PortB Termination override.*
  - UINT8 [PchSkyCamPortCTermOvrEnable](#)  
*Offset 0x02FD - Enable SkyCam PortC Termination override Enable/disable PortC Termination override.*
-

- UINT8 [PchSkyCamPortDTermOvrEnable](#)  
*Offset 0x02FE - Enable SkyCam PortD Termination override Enable/disable PortD Termination override.*
  - UINT8 [PchSkyCamPortATrimEnable](#)  
*Offset 0x02FF - Enable SkyCam PortA Clk Trim Enable/disable PortA Clk Trim.*
  - UINT8 [PchSkyCamPortBTrimEnable](#)  
*Offset 0x0300 - Enable SkyCam PortB Clk Trim Enable/disable PortB Clk Trim.*
  - UINT8 [PchSkyCamPortCTrimEnable](#)  
*Offset 0x0301 - Enable SkyCam PortC Clk Trim Enable/disable PortC Clk Trim.*
  - UINT8 [PchSkyCamPortDTrimEnable](#)  
*Offset 0x0302 - Enable SkyCam PortD Clk Trim Enable/disable PortD Clk Trim.*
  - UINT8 [PchSkyCamPortACtleEnable](#)  
*Offset 0x0303 - Enable SkyCam PortA Ctle Enable/disable PortA Ctle.*
  - UINT8 [PchSkyCamPortBCtleEnable](#)  
*Offset 0x0304 - Enable SkyCam PortB Ctle Enable/disable PortB Ctle.*
  - UINT8 [PchSkyCamPortCDCtleEnable](#)  
*Offset 0x0305 - Enable SkyCam PortCD Ctle Enable/disable PortCD Ctle.*
  - UINT8 [PchSkyCamPortACtleCapValue](#)  
*Offset 0x0306 - Enable SkyCam PortA Ctle Cap Value Enable/disable PortA Ctle Cap Value.*
  - UINT8 [PchSkyCamPortBCtleCapValue](#)  
*Offset 0x0307 - Enable SkyCam PortB Ctle Cap Value Enable/disable PortB Ctle Cap Value.*
  - UINT8 [PchSkyCamPortCDCtleCapValue](#)  
*Offset 0x0308 - Enable SkyCam PortCD Ctle Cap Value Enable/disable PortCD Ctle Cap Value.*
  - UINT8 [PchSkyCamPortACtleResValue](#)  
*Offset 0x0309 - Enable SkyCam PortA Ctle Res Value Enable/disable PortA Ctle Res Value.*
  - UINT8 [PchSkyCamPortBCtleResValue](#)  
*Offset 0x030A - Enable SkyCam PortB Ctle Res Value Enable/disable PortB Ctle Res Value.*
  - UINT8 [PchSkyCamPortCDCtleResValue](#)  
*Offset 0x030B - Enable SkyCam PortCD Ctle Res Value Enable/disable PortCD Ctle Res Value.*
  - UINT8 [PchSkyCamPortAClkTrimValue](#)  
*Offset 0x030C - Enable SkyCam PortA Clk Trim Value Enable/disable PortA Clk Trim Value.*
  - UINT8 [PchSkyCamPortBClkTrimValue](#)  
*Offset 0x030D - Enable SkyCam PortB Clk Trim Value Enable/disable PortB Clk Trim Value.*
  - UINT8 [PchSkyCamPortCClkTrimValue](#)  
*Offset 0x030E - Enable SkyCam PortC Clk Trim Value Enable/disable PortC Clk Trim Value.*
  - UINT8 [PchSkyCamPortDClkTrimValue](#)  
*Offset 0x030F - Enable SkyCam PortD Clk Trim Value Enable/disable PortD Clk Trim Value.*
  - UINT16 [PchSkyCamPortADataTrimValue](#)  
*Offset 0x0310 - Enable SkyCam Port A Data Trim Value Enable/disable Port A Data Trim Value.*
  - UINT16 [PchSkyCamPortBDataTrimValue](#)  
*Offset 0x0312 - Enable SkyCam Port B Data Trim Value Enable/disable Port B Data Trim Value.*
  - UINT16 [PchSkyCamPortCDDDataTrimValue](#)  
*Offset 0x0314 - Enable SkyCam C/D Data Trim Value Enable/disable C/D Data Trim Value.*
  - UINT8 [PchDmiAspm](#)  
*Offset 0x0316 - Enable DMI ASPM ASPM on PCH side of the DMI Link.*
  - UINT8 [PchPwrOptEnable](#)  
*Offset 0x0317 - Enable Power Optimizer Enable DMI Power Optimizer on PCH side.*
  - UINT8 [PchWriteProtectionEnable](#) [5]  
*Offset 0x0318 - PCH Flash Protection Ranges Write Enable Write or erase is blocked by hardware.*
  - UINT8 [PchReadProtectionEnable](#) [5]  
*Offset 0x031D - PCH Flash Protection Ranges Read Enable Read is blocked by hardware.*
  - UINT16 [PchProtectedRangeLimit](#) [5]
-



Offset 0x0322 - PCH Protect Range Limit Left shifted address by 12 bits with address bits 11:0 are assumed to be FFFh for limit comparison.

- UINT16 [PchProtectedRangeBase](#) [5]  
Offset 0x032C - PCH Protect Range Base Left shifted address by 12 bits with address bits 11:0 are assumed to be 0.
- UINT8 [PchHdaPme](#)  
Offset 0x0336 - Enable Pme Enable Azalia wake-on-ring.
- UINT8 [PchHdaIoBufferVoltage](#)  
Offset 0x0337 - IO Buffer Voltage I/O Buffer Voltage Mode Select: 0: 3.3V, 1: 1.8V.
- UINT8 [PchHdaVcType](#)  
Offset 0x0338 - VC Type Virtual Channel Type Select: 0: VC0, 1: VC1.
- UINT8 [PchHdaLinkFrequency](#)  
Offset 0x0339 - HD Audio Link Frequency HDA Link Freq (PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 0: 6MHz, 1: 12MHz, 2: 24MHz.
- UINT8 [PchHdaIDispLinkFrequency](#)  
Offset 0x033A - iDisp-Link Frequency iDisp-Link Freq (PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 4: 96MHz, 3: 48MHz.
- UINT8 [PchHdaIDispLinkTmode](#)  
Offset 0x033B - iDisp-Link T-mode iDisp-Link T-Mode (PCH\_HDAUDIO\_IDISP\_TMODE enum): 0: 2T, 1: 1T.
- UINT8 [PchHdaDspUaaCompliance](#)  
Offset 0x033C - Universal Audio Architecture compliance for DSP enabled system 0: Not-UAA Compliant (Intel SST driver supported only), 1: UAA Compliant (HDA Inbox driver or SST driver supported).
- UINT8 [PchHdaIDispCodecDisconnect](#)  
Offset 0x033D - iDisplay Audio Codec disconnection 0: Not disconnected, enumerable, 1: Disconnected SDI, not enumerable.
- UINT8 [PchHdaDspEndpointDmic](#)  
Offset 0x033E - DSP DMIC Select (PCH\_HDAUDIO\_DMIC\_TYPE enum) 0: Disable; 1: 2ch array; 2: 4ch array; 3: 1ch array.
- UINT8 [PchHdaDspEndpointBluetooth](#)  
Offset 0x033F - DSP Bluetooth enablement 0: Disable; 1: Enable.
- UINT32 [PchHdaDspFeatureMask](#)  
Offset 0x0340 - Bitmask of supported DSP features [BIT0] - WoV; [BIT1] - BT Sideband; [BIT2] - Codec VAD; [BIT5] - BT Intel HFP; [BIT6].
- UINT32 [PchHdaDspPpModuleMask](#)  
Offset 0x0344 - Bitmask of supported DSP Pre/Post-Processing Modules Deprecated: Specific pre/post-processing module bit position must be coherent with the ACPI implementation: \_SB.PCI0.HDAS.\_DSM Function 3: Query Pre/Post Processing Module Support.
- UINT8 [PchHdaDspEndpointI2s](#)  
Offset 0x0348 - DSP I2S enablement 0: Disable; 1: Enable.
- UINT8 [PchIoApicBdfValid](#)  
Offset 0x0349 - Enable PCH Io Apic Set to 1 if BDF value is valid.
- UINT8 [PchIoApicBusNumber](#)  
Offset 0x034A - PCH Io Apic Bus Number Bus/Device/Function used as Requestor / Completer ID.
- UINT8 [PchIoApicDeviceNumber](#)  
Offset 0x034B - PCH Io Apic Device Number Bus/Device/Function used as Requestor / Completer ID.
- UINT8 [PchIoApicFunctionNumber](#)  
Offset 0x034C - PCH Io Apic Function Number Bus/Device/Function used as Requestor / Completer ID.
- UINT8 [PchIoApicEntry24\\_119](#)  
Offset 0x034D - Enable PCH Io Apic Entry 24-119 0: Disable; 1: Enable.
- UINT8 [PchIoApicId](#)  
Offset 0x034E - PCH Io Apic ID This member determines IOAPIC ID.
- UINT8 [PchIoApicRangeSelect](#)  
Offset 0x034F - PCH Io Apic Range Select Define address bits 19:12 for the IOxAPIC range.
- UINT8 [PchIshSpiGpioAssign](#)

- Offset 0x0350 - Enable PCH ISH SPI GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshUart0GpioAssign](#)
  - Offset 0x0351 - Enable PCH ISH UART0 GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshUart1GpioAssign](#)
  - Offset 0x0352 - Enable PCH ISH UART1 GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshI2c0GpioAssign](#)
  - Offset 0x0353 - Enable PCH ISH I2C0 GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshI2c1GpioAssign](#)
  - Offset 0x0354 - Enable PCH ISH I2C1 GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshI2c2GpioAssign](#)
  - Offset 0x0355 - Enable PCH ISH I2C2 GPIO pins assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp0GpioAssign](#)
  - Offset 0x0356 - Enable PCH ISH GP\_0 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp1GpioAssign](#)
  - Offset 0x0357 - Enable PCH ISH GP\_1 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp2GpioAssign](#)
  - Offset 0x0358 - Enable PCH ISH GP\_2 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp3GpioAssign](#)
  - Offset 0x0359 - Enable PCH ISH GP\_3 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp4GpioAssign](#)
  - Offset 0x035A - Enable PCH ISH GP\_4 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp5GpioAssign](#)
  - Offset 0x035B - Enable PCH ISH GP\_5 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp6GpioAssign](#)
  - Offset 0x035C - Enable PCH ISH GP\_6 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshGp7GpioAssign](#)
  - Offset 0x035D - Enable PCH ISH GP\_7 GPIO pin assigned 0: Disable; 1: Enable.*

    - UINT8 [PchIshPdtUnlock](#)
  - Offset 0x035E - PCH ISH PDT Unlock Msg 0: False; 1: True.*

    - UINT8 [PchLanLtrEnable](#)
  - Offset 0x035F - Enable PCH Lan LTR capability of PCH internal LAN 0: Disable; 1: Enable.*

    - UINT8 [PchLanK1OffEnable](#)
  - Offset 0x0360 - Enable PCH Lan use CLKREQ for GbE power management 0: Disable; 1: Enable.*

    - UINT8 [PchLanClkReqSupported](#)
  - Offset 0x0361 - Indicate whether dedicated CLKREQ# is supported 0: Disable; 1: Enable.*

    - UINT8 [PchLanClkReqNumber](#)
  - Offset 0x0362 - CLKREQ# used by GbE Valid if ClkReqSupported is TRUE.*

    - UINT8 [PchLockDownBiosLock](#)
  - Offset 0x0363 - Enable LOCKDOWN BIOS LOCK Enable the BIOS Lock feature and set EISS bit (D31:F5:RegD←→Ch[5]) for the BIOS region protection.*

    - UINT8 [PchLockDownSpiEiss](#)
  - Offset 0x0364 - Enable LOCKDOWN SPI Eiss Enable InSMM.STS (EISS) in SPI.*

    - UINT8 [PchCrid](#)
  - Offset 0x0365 - PCH Compatibility Revision ID This member describes whether or not the CRID feature of PCH should be enabled.*

    - UINT16 [PchSubSystemVendorId](#)
  - Offset 0x0366 - PCH Sub system vendor ID Default Subsystem Vendor ID of the PCH devices.*

    - UINT16 [PchSubSystemId](#)
  - Offset 0x0368 - PCH Sub system ID Default Subsystem ID of the PCH devices.*

    - UINT8 [PchLegacyIoLowLatency](#)
  - Offset 0x036A - PCH Legacy IO Low Latency Enable todo \$EN\_DIS.*
-

- UINT8 [UnusedUpdSpace15](#) [5]  
*Offset 0x036B.*
- UINT8 [PcieRpHotPlug](#) [24]  
*Offset 0x0370 - Enable PCIE RP HotPlug Indicate whether the root port is hot plug available.*
- UINT8 [PcieRpPmSci](#) [24]  
*Offset 0x0388 - Enable PCIE RP Pm Sci Indicate whether the root port power manager SCI is enabled.*
- UINT8 [PcieRpExtSync](#) [24]  
*Offset 0x03A0 - Enable PCIE RP Ext Sync Indicate whether the extended synch is enabled.*
- UINT8 [PcieRpTransmitterHalfSwing](#) [24]  
*Offset 0x03B8 - Enable PCIE RP Transmitter Half Swing Indicate whether the Transmitter Half Swing is enabled.*
- UINT8 [PcieRpClkReqDetect](#) [24]  
*Offset 0x03D0 - Enable PCIE RP Clk Req Detect Probe CLKREQ# signal before enabling CLKREQ# based power management.*
- UINT8 [PcieRpAdvancedErrorReporting](#) [24]  
*Offset 0x03E8 - PCIE RP Advanced Error Report Indicate whether the Advanced Error Reporting is enabled.*
- UINT8 [PcieRpUnsupportedRequestReport](#) [24]  
*Offset 0x0400 - PCIE RP Unsupported Request Report Indicate whether the Unsupported Request Report is enabled.*
- UINT8 [PcieRpFatalErrorReport](#) [24]  
*Offset 0x0418 - PCIE RP Fatal Error Report Indicate whether the Fatal Error Report is enabled.*
- UINT8 [PcieRpNoFatalErrorReport](#) [24]  
*Offset 0x0430 - PCIE RP No Fatal Error Report Indicate whether the No Fatal Error Report is enabled.*
- UINT8 [PcieRpCorrectableErrorReport](#) [24]  
*Offset 0x0448 - PCIE RP Correctable Error Report Indicate whether the Correctable Error Report is enabled.*
- UINT8 [PcieRpSystemErrorOnFatalError](#) [24]  
*Offset 0x0460 - PCIE RP System Error On Fatal Error Indicate whether the System Error on Fatal Error is enabled.*
- UINT8 [PcieRpSystemErrorOnNonFatalError](#) [24]  
*Offset 0x0478 - PCIE RP System Error On Non Fatal Error Indicate whether the System Error on Non Fatal Error is enabled.*
- UINT8 [PcieRpSystemErrorOnCorrectableError](#) [24]  
*Offset 0x0490 - PCIE RP System Error On Correctable Error Indicate whether the System Error on Correctable Error is enabled.*
- UINT8 [PcieRpMaxPayload](#) [24]  
*Offset 0x04A8 - PCIE RP Max Payload Max Payload Size supported, Default 128B, see enum PCH\_PCIE\_MAX\_↔PAYLOAD.*
- UINT8 [PcieRpDeviceResetPadActiveHigh](#) [24]  
*Offset 0x04C0 - PCIE RP Device Reset Pad Active High Indicated whether PERST# is active 0: Low; 1: High, See: DeviceResetPad.*
- UINT8 [PcieRpPcieSpeed](#) [24]  
*Offset 0x04D8 - PCIE RP Pcie Speed Determines each PCIE Port speed capability.*
- UINT8 [PcieRpGen3EqPh3Method](#) [24]  
*Offset 0x04F0 - PCIE RP Gen3 Equalization Phase Method PCIe Gen3 Eq Ph3 Method (see PCH\_PCIE\_EQ\_ME↔THOD).*
- UINT8 [PcieRpPhysicalSlotNumber](#) [24]  
*Offset 0x0508 - PCIE RP Physical Slot Number Indicates the slot number for the root port.*
- UINT8 [PcieRpCompletionTimeout](#) [24]  
*Offset 0x0520 - PCIE RP Completion Timeout The root port completion timeout(see: PCH\_PCIE\_COMPLETION\_↔TIMEOUT).*
- UINT32 [PcieRpDeviceResetPad](#) [24]  
*Offset 0x0538 - PCIE RP Device Reset Pad The PCH pin assigned to device PERST# signal if available, zero otherwise.*
- UINT8 [PcieRpAspm](#) [24]  
*Offset 0x0598 - PCIE RP Aspm The ASPM configuration of the root port (see: PCH\_PCIE\_ASPM\_CONTROL).*

- UINT8 [PcieRpL1Substates](#) [24]  
*Offset 0x05B0 - PCIE RP L1 Substates The L1 Substates configuration of the root port (see: PCH\_PCIE\_L1SUBSTATES\_CONTROL).*
  - UINT8 [PcieRpLtrEnable](#) [24]  
*Offset 0x05C8 - PCIE RP Ltr Enable Latency Tolerance Reporting Mechanism.*
  - UINT8 [PcieRpLtrConfigLock](#) [24]  
*Offset 0x05E0 - PCIE RP Ltr Config Lock 0: Disable; 1: Enable.*
  - UINT8 [PcieEqPh3LaneParamCm](#) [24]  
*Offset 0x05F8 - PCIE Eq Ph3 Lane Param Cm PCH\_PCIE\_EQ\_LANE\_PARAM.*
  - UINT8 [PcieEqPh3LaneParamCp](#) [24]  
*Offset 0x0610 - PCIE Eq Ph3 Lane Param Cp PCH\_PCIE\_EQ\_LANE\_PARAM.*
  - UINT8 [PcieSwEqCoeffListCm](#) [5]  
*Offset 0x0628 - PCIE Sw Eq CoeffList Cm PCH\_PCIE\_EQ\_PARAM.*
  - UINT8 [PcieSwEqCoeffListCp](#) [5]  
*Offset 0x062D - PCIE Sw Eq CoeffList Cp PCH\_PCIE\_EQ\_PARAM.*
  - UINT8 [PcieDisableRootPortClockGating](#)  
*Offset 0x0632 - PCIE Disable RootPort Clock Gating Describes whether the PCI Express Clock Gating for each root port is enabled by platform modules.*
  - UINT8 [PcieEnablePeerMemoryWrite](#)  
*Offset 0x0633 - PCIE Enable Peer Memory Write This member describes whether Peer Memory Writes are enabled on the platform.*
  - UINT8 [PcieAllowNoLtrIccPllShutdown](#)  
*Offset 0x0634 - PCIE Allow No Ltr Icc PLL Shutdown Allows BIOS to control ICC PLL Shutdown by determining PCIe devices are LTR capable or leaving untouched.*
  - UINT8 [PcieComplianceTestMode](#)  
*Offset 0x0635 - PCIE Compliance Test Mode Compliance Test Mode shall be enabled when using Compliance Load Board.*
  - UINT16 [PcieDetectTimeoutMs](#)  
*Offset 0x0636 - PCIE Rp Detect Timeout Ms Will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.*
  - UINT8 [PcieRpFunctionSwap](#)  
*Offset 0x0638 - PCIE Rp Function Swap Allows BIOS to use root port function number swapping when root port of function 0 is disabled.*
  - UINT8 [PchPmPmeB0S5Dis](#)  
*Offset 0x0639 - PCH Pm PME\_B0\_S5\_DIS When cleared (default), wake events from PME\_B0\_STS are allowed in S5 if PME\_B0\_EN = 1.*
  - UINT8 [PchPmSlpS0VmEnable](#)  
*Offset 0x063A - PCH Pm Slp S0 Voltage Margining Enable Indicates platform has support for VCCPrim\_Core Voltage Margining in SLP\_S0# asserted state.*
  - UINT8 [UnusedUpdSpace16](#) [5]  
*Offset 0x063B.*
  - UINT8 [PchPmWolEnableOverride](#)  
*Offset 0x0640 - PCH Pm Wol Enable Override Corresponds to the WOL Enable Override bit in the General PM Configuration B (GEN\_PMCON\_B) register.*
  - UINT8 [PchPmPcieWakeFromDeepSx](#)  
*Offset 0x0641 - PCH Pm Pcie Wake From DeepSx Determine if enable PCIe to wake from deep Sx.*
  - UINT8 [PchPmWoWlanEnable](#)  
*Offset 0x0642 - PCH Pm WoW lan Enable Determine if WLAN wake from Sx, corresponds to the HOST\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.*
  - UINT8 [PchPmWoWlanDeepSxEnable](#)  
*Offset 0x0643 - PCH Pm WoW lan DeepSx Enable Determine if WLAN wake from DeepSx, corresponds to the DSX\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.*
  - UINT8 [PchPmLanWakeFromDeepSx](#)
-

- Offset 0x0644 - PCH Pm Lan Wake From DeepSx Determine if enable LAN to wake from deep Sx.

  - UINT8 [PchPmDeepSxPol](#)
- Offset 0x0645 - PCH Pm Deep Sx Pol Deep Sx Policy.

  - UINT8 [PchPmSlpS3MinAssert](#)
- Offset 0x0646 - PCH Pm Slp S3 Min Assert SLP\_S3 Minimum Assertion Width Policy.

  - UINT8 [PchPmSlpS4MinAssert](#)
- Offset 0x0647 - PCH Pm Slp S4 Min Assert SLP\_S4 Minimum Assertion Width Policy.

  - UINT8 [PchPmSlpSusMinAssert](#)
- Offset 0x0648 - PCH Pm Slp Sus Min Assert SLP\_SUS Minimum Assertion Width Policy.

  - UINT8 [PchPmSlpAMinAssert](#)
- Offset 0x0649 - PCH Pm Slp A Min Assert SLP\_A Minimum Assertion Width Policy.

  - UINT8 [UnusedUpdSpace17](#) [6]
- Offset 0x064A.

  - UINT8 [PchPmLpcClockRun](#)
- Offset 0x0650 - PCH Pm Lpc Clock Run This member describes whether or not the LPC ClockRun feature of PCH should be enabled.

  - UINT8 [PchPmSlpStrchSusUp](#)
- Offset 0x0651 - PCH Pm Slp Strch Sus Up Enable SLP\_X Stretching After SUS Well Power Up.

  - UINT8 [PchPmSlpLanLowDc](#)
- Offset 0x0652 - PCH Pm Slp Lan Low Dc Enable/Disable SLP\_LAN# Low on DC Power.

  - UINT8 [PchPmPwrBtnOverridePeriod](#)
- Offset 0x0653 - PCH Pm Pwr Btn Override Period PCH power button override period.

  - UINT8 [PchPmDisableDsxAcPresentPulldown](#)
- Offset 0x0654 - PCH Pm Disable Dsx Ac Present Pulldown When Disable, PCH will internal pull down AC\_PRESENT in deep SX and during G3 exit.

  - UINT8 [PchPmCapsuleResetType](#)
- Offset 0x0655 - PCH Pm Capsule Reset Type Deprecated: Determines type of reset issued during UpdateCapsule().

  - UINT8 [PchPmDisableNativePowerButton](#)
- Offset 0x0656 - PCH Pm Disable Native Power Button Power button native mode disable.

  - UINT8 [PchPmSlpS0Enable](#)
- Offset 0x0657 - PCH Pm Slp S0 Enable Indicates whether SLP\_S0# is to be asserted when PCH reaches idle state.

  - UINT8 [PchPmMeWakeSts](#)
- Offset 0x0658 - PCH Pm ME\_WAKE\_STS Clear the ME\_WAKE\_STS bit in the Power and Reset Status (PRSTS) register.

  - UINT8 [PchPmWolOvrWkSts](#)
- Offset 0x0659 - PCH Pm WOL\_OVR\_WK\_STS Clear the WOL\_OVR\_WK\_STS bit in the Power and Reset Status (PRSTS) register.

  - UINT8 [PchPmPwrCycDur](#)
- Offset 0x065A - PCH Pm Reset Power Cycle Duration Could be customized in the unit of second.

  - UINT8 [UnusedUpdSpace18](#)
- Offset 0x065B.

  - UINT8 [PchPort61hEnable](#)
- Offset 0x065C - PCH Port 61h Config Enable/Disable Used for the emulation feature for Port61h read.

  - UINT8 [SataPwrOptEnable](#)
- Offset 0x065D - PCH Sata Pwr Opt Enable SATA Power Optimizer on PCH side.

  - UINT8 [EsataSpeedLimit](#)
- Offset 0x065E - PCH Sata eSATA Speed Limit When enabled, BIOS will configure the PxSCTL.SPD to 2 to limit the eSATA port speed.

  - UINT8 [SataSpeedLimit](#)
- Offset 0x065F - PCH Sata Speed Limit Indicates the maximum speed the SATA controller can support 0h: Pch↔SataSpeedDefault.

  - UINT8 [SataPortsHotPlug](#) [8]

- Offset 0x0660 - Enable SATA Port HotPlug Enable SATA Port HotPlug.*

    - UINT8 [SataPortsInterlockSw](#) [8]
 

*Offset 0x0668 - Enable SATA Port Interlock Sw Enable SATA Port Interlock Sw.*
    - UINT8 [SataPortsExternal](#) [8]
 

*Offset 0x0670 - Enable SATA Port External Enable SATA Port External.*
    - UINT8 [SataPortsSpinUp](#) [8]
 

*Offset 0x0678 - Enable SATA Port SpinUp Enable the COMRESET initialization Sequence to the device.*
    - UINT8 [SataPortsSolidStateDrive](#) [8]
 

*Offset 0x0680 - Enable SATA Port Solid State Drive 0: HDD; 1: SSD.*
    - UINT8 [SataPortsEnableDitoConfig](#) [8]
 

*Offset 0x0688 - Enable SATA Port Enable Dito Config Enable DEVSLP Idle Timeout settings (DmVal, DitoVal).*
    - UINT8 [SataPortsDmVal](#) [8]
 

*Offset 0x0690 - Enable SATA Port DmVal DITO multiplier.*
    - UINT16 [SataPortsDitoVal](#) [8]
 

*Offset 0x0698 - Enable SATA Port DmVal DEVSLP Idle Timeout (DITO), Default is 625.*
    - UINT8 [SataPortsZpOdd](#) [8]
 

*Offset 0x06A8 - Enable SATA Port ZpOdd Support zero power ODD.*
    - UINT8 [SataRstRaidAlternateId](#)

*Offset 0x06B0 - PCH Sata Rst Raid Alternate Id Enable RAID Alternate ID.*
    - UINT8 [SataRstRaid0](#)

*Offset 0x06B1 - PCH Sata Rst Raid0 RAID0.*
    - UINT8 [SataRstRaid1](#)

*Offset 0x06B2 - PCH Sata Rst Raid1 RAID1.*
    - UINT8 [SataRstRaid10](#)

*Offset 0x06B3 - PCH Sata Rst Raid10 RAID10.*
    - UINT8 [SataRstRaid5](#)

*Offset 0x06B4 - PCH Sata Rst Raid5 RAID5.*
    - UINT8 [SataRstIrrt](#)

*Offset 0x06B5 - PCH Sata Rst Irrt Intel Rapid Recovery Technology.*
    - UINT8 [SataRstOromUiBanner](#)

*Offset 0x06B6 - PCH Sata Rst Orom Ui Banner OROM UI and BANNER.*
    - UINT8 [SataRstOromUiDelay](#)

*Offset 0x06B7 - PCH Sata Rst Orom Ui Delay 00b: 2 secs; 01b: 4 secs; 10b: 6 secs; 11: 8 secs (see: PCH\_SATA\_OROM\_DELAY).*
    - UINT8 [SataRstHddUnlock](#)

*Offset 0x06B8 - PCH Sata Rst Hdd Unlock Indicates that the HDD password unlock in the OS is enabled.*
    - UINT8 [SataRstLedLocate](#)

*Offset 0x06B9 - PCH Sata Rst Led Locate Indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.*
    - UINT8 [SataRstIrrtOnly](#)

*Offset 0x06BA - PCH Sata Rst Irrt Only Allow only IRRT drives to span internal and external ports.*
    - UINT8 [SataRstSmartStorage](#)

*Offset 0x06BB - PCH Sata Rst Smart Storage RST Smart Storage caching Bit.*
    - UINT8 [SataRstPcieEnable](#) [3]
 

*Offset 0x06BC - PCH Sata Rst Pcie Storage Remap enable Enable Intel RST for PCIe Storage remapping.*
    - UINT8 [SataRstPcieStoragePort](#) [3]
 

*Offset 0x06BF - PCH Sata Rst Pcie Storage Port Intel RST for PCIe Storage remapping - PCIe Port Selection (1-based, 0 = autodetect).*
    - UINT8 [SataRstPcieDeviceResetDelay](#) [3]
 

*Offset 0x06C2 - PCH Sata Rst Pcie Device Reset Delay PCIe Storage Device Reset Delay in milliseconds.*
    - UINT8 [PchScsEmmcHs400TuningRequired](#)
-

- Offset 0x06C5 - Enable eMMC HS400 Training Determine if HS400 Training is required.*

    - UINT8 [PchScsEmmcHs400DIIDataValid](#)
  - Offset 0x06C6 - Set HS400 Tuning Data Valid Set if HS400 Tuning Data Valid.*

    - UINT8 [PchScsEmmcHs400RxStrobeDII1](#)
  - Offset 0x06C7 - Rx Strobe Delay Control Rx Strobe Delay Control - Rx Strobe Delay DLL 1 (HS400 Mode).*

    - UINT8 [PchScsEmmcHs400TxDataDII](#)
  - Offset 0x06C8 - Tx Data Delay Control Tx Data Delay Control 1 - Tx Data Delay (HS400 Mode).*

    - UINT8 [PchScsEmmcHs400DriverStrength](#)
  - Offset 0x06C9 - I/O Driver Strength I/O driver strength: 0 - 33 Ohm, 1 - 40 Ohm, 2 - 50 Ohm.*

    - UINT8 [SerialIoGpio](#)
  - Offset 0x06CA - Enable Pch Serial IO GPIO Determines if enable Serial IO GPIO.*

    - UINT8 [SerialIoI2cVoltage](#) [6]
  - Offset 0x06CB - IO voltage for I2C controllers Selects the IO voltage for I2C controllers, 0: PchSerialIoI2c33V, 1: PchSerialIoI2c18V.*

    - UINT8 [SerialIoSpiCsPolarity](#) [2]
  - Offset 0x06D1 - SPI ChipSelect signal polarity Selects SPI ChipSelect signal polarity.*

    - UINT8 [SerialIoUartHwFlowCtrl](#) [3]
  - Offset 0x06D3 - Enables UART hardware flow control, CTS and RTS lines Enables UART hardware flow control, CTS and RTS linesh.*

    - UINT8 [SerialIoDebugUartNumber](#)
  - Offset 0x06D6 - UART Number For Debug Purpose UART number for debug purpose.*

    - UINT8 [SerialIoEnableDebugUartAfterPost](#)
  - Offset 0x06D7 - Enable Debug UART Controller Enable debug UART controller after post.*

    - UINT8 [PchSirqEnable](#)
  - Offset 0x06D8 - Enable Serial IRQ Determines if enable Serial IRQ.*

    - UINT8 [PchSirqMode](#)
  - Offset 0x06D9 - Serial IRQ Mode Select Serial IRQ Mode Select, 0: quiet mode, 1: continuous mode.*

    - UINT8 [PchStartFramePulse](#)
  - Offset 0x06DA - Start Frame Pulse Width Start Frame Pulse Width, 0: PchSfpw4Clk, 1: PchSfpw6Clk, 2: PchSfpw8Clk.*

    - UINT8 [PchThermalDeviceEnable](#)
  - Offset 0x06DB - Enable Thermal Device Enable Thermal Device.*

    - UINT16 [PchT0Level](#)
  - Offset 0x06DC - Thermal Throttling Customized T0Level Value Customized T0Level value.*

    - UINT16 [PchT1Level](#)
  - Offset 0x06DE - Thermal Throttling Customized T1Level Value Customized T1Level value.*

    - UINT16 [PchT2Level](#)
  - Offset 0x06E0 - Thermal Throttling Customized T2Level Value Customized T2Level value.*

    - UINT8 [PchTsmicLock](#)
  - Offset 0x06E2 - Thermal Device SMI Enable This locks down SMI Enable on Alert Thermal Sensor Trip.*

    - UINT8 [PchTTEnable](#)
  - Offset 0x06E3 - Enable The Thermal Throttle Enable the thermal throttle function.*

    - UINT8 [PchTTState13Enable](#)
  - Offset 0x06E4 - PMSync State 13 When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 will force at least T2 state.*

    - UINT8 [PchTTLock](#)
  - Offset 0x06E5 - Thermal Throttle Lock Thermal Throttle Lock.*

    - UINT8 [TTSuggestedSetting](#)
  - Offset 0x06E6 - Thermal Throttling Suggested Setting Thermal Throttling Suggested Setting.*

    - UINT8 [TTCrossThrottling](#)
  - Offset 0x06E7 - Enable PCH Cross Throttling Enable/Disable PCH Cross Throttling \$EN\_DIS.*
-



- UINT8 [PchDmiTsawEn](#)  
*Offset 0x06E8 - DMI Thermal Sensor Autonomous Width Enable DMI Thermal Sensor Autonomous Width Enable.*
  - UINT8 [DmiSuggestedSetting](#)  
*Offset 0x06E9 - DMI Thermal Sensor Suggested Setting DMT thermal sensor suggested representative values.*
  - UINT8 [DmiTS0TW](#)  
*Offset 0x06EA - Thermal Sensor 0 Target Width Thermal Sensor 0 Target Width.*
  - UINT8 [DmiTS1TW](#)  
*Offset 0x06EB - Thermal Sensor 1 Target Width Thermal Sensor 1 Target Width.*
  - UINT8 [DmiTS2TW](#)  
*Offset 0x06EC - Thermal Sensor 2 Target Width Thermal Sensor 2 Target Width.*
  - UINT8 [DmiTS3TW](#)  
*Offset 0x06ED - Thermal Sensor 3 Target Width Thermal Sensor 3 Target Width.*
  - UINT8 [SataP0T1M](#)  
*Offset 0x06EE - Port 0 T1 Multiplier Port 0 T1 Multiplier.*
  - UINT8 [SataP0T2M](#)  
*Offset 0x06EF - Port 0 T2 Multiplier Port 0 T2 Multiplier.*
  - UINT8 [SataP0T3M](#)  
*Offset 0x06F0 - Port 0 T3 Multiplier Port 0 T3 Multiplier.*
  - UINT8 [SataP0TDisp](#)  
*Offset 0x06F1 - Port 0 Tdispatch Port 0 Tdispatch.*
  - UINT8 [SataP1T1M](#)  
*Offset 0x06F2 - Port 1 T1 Multiplier Port 1 T1 Multiplier.*
  - UINT8 [SataP1T2M](#)  
*Offset 0x06F3 - Port 1 T2 Multiplier Port 1 T2 Multiplier.*
  - UINT8 [SataP1T3M](#)  
*Offset 0x06F4 - Port 1 T3 Multiplier Port 1 T3 Multiplier.*
  - UINT8 [SataP1TDisp](#)  
*Offset 0x06F5 - Port 1 Tdispatch Port 1 Tdispatch.*
  - UINT8 [SataP0Tinact](#)  
*Offset 0x06F6 - Port 0 Tinactive Port 0 Tinactive.*
  - UINT8 [SataP0TDispFinit](#)  
*Offset 0x06F7 - Port 0 Alternate Fast Init Tdispatch Port 0 Alternate Fast Init Tdispatch.*
  - UINT8 [SataP1Tinact](#)  
*Offset 0x06F8 - Port 1 Tinactive Port 1 Tinactive.*
  - UINT8 [SataP1TDispFinit](#)  
*Offset 0x06F9 - Port 1 Alternate Fast Init Tdispatch Port 1 Alternate Fast Init Tdispatch.*
  - UINT8 [SataThermalSuggestedSetting](#)  
*Offset 0x06FA - Sata Thermal Throttling Suggested Setting Sata Thermal Throttling Suggested Setting.*
  - UINT8 [PchMemoryThrottlingEnable](#)  
*Offset 0x06FB - Enable Memory Thermal Throttling Enable Memory Thermal Throttling.*
  - UINT8 [PchMemoryPmsyncEnable](#) [2]  
*Offset 0x06FC - Memory Thermal Throttling Enable Memory Thermal Throttling.*
  - UINT8 [PchMemoryC0TransmitEnable](#) [2]  
*Offset 0x06FE - Enable Memory Thermal Throttling Enable Memory Thermal Throttling.*
  - UINT8 [PchMemoryPinSelection](#) [2]  
*Offset 0x0700 - Enable Memory Thermal Throttling Enable Memory Thermal Throttling.*
  - UINT16 [PchTemperatureHotLevel](#)  
*Offset 0x0702 - Thermal Device Temperature Decides the temperature.*
  - UINT8 [PchDisableComplianceMode](#)  
*Offset 0x0704 - Disable XHCI Compliance Mode This policy will disable XHCI compliance mode on all ports.*
  - UINT8 [Usb2OverCurrentPin](#) [16]
-



- Offset 0x0705 - USB2 Port Over Current Pin Describe the specific over current pin number of USB 2.0 Port N.*

    - UINT8 [Usb3OverCurrentPin](#) [10]
  - Offset 0x0715 - USB3 Port Over Current Pin Describe the specific over current pin number of USB 3.0 Port N.*

    - UINT8 [Early8254ClockGatingEnable](#)
  - Offset 0x071F - Enable 8254 Static Clock Gating in early POST time Set 8254CGE=1 is required for C11 support.*

    - UINT8 [SataRstOptaneMemory](#)
  - Offset 0x0720 - PCH Sata Rst Optane Memory Optane Memory \$EN\_DIS.*

    - UINT8 [SataRstCpuAttachedStorage](#)
  - Offset 0x0721 - PCH SATA RST CPU attached storage RST CPU attached storage \$EN\_DIS.*

    - UINT8 [HybridStorageMode](#)
  - Offset 0x0722 - Hybrid Storage Mode Enables support for Hybrid storage devices.*

    - UINT8 [UnusedUpdSpace19](#)
  - Offset 0x0723.*

    - UINT32 [PchPcieDeviceOverrideTablePtr](#)
  - Offset 0x0724 - Pch PCIE device override table pointer The PCIe device table is being used to override PCIe device ASPM settings.*

    - UINT8 [EnableTcoTimer](#)
  - Offset 0x0728 - Enable TCO timer.*

    - UINT8 [EcCmdProvisionEav](#)
  - Offset 0x0729 - EcCmdProvisionEav Ephemeral Authorization Value default values.*

    - UINT8 [EcCmdLock](#)
  - Offset 0x072A - EcCmdLock EcCmdLock default values.*

    - UINT8 [UnusedUpdSpace20](#) [5]
  - Offset 0x072B.*

    - UINT64 [SendEcCmd](#)
  - Offset 0x0730 - SendEcCmd SendEcCmd function pointer.*

    - UINT64 [BgpdtHash](#) [4]
  - Offset 0x0738 - BgpdtHash[4] BgpdtHash values.*

    - UINT64 [BiosGuardModulePtr](#)
  - Offset 0x0758 - BiosGuardModulePtr BiosGuardModulePtr default values.*

    - UINT32 [BiosGuardAttr](#)
  - Offset 0x0760 - BiosGuardAttr BiosGuardAttr default values.*

    - UINT8 [SgxSinitNvsData](#)
  - Offset 0x0764 - SgxSinitNvsData SgxSinitNvsData default values.*

    - UINT8 [UnusedUpdSpace21](#) [3]
  - Offset 0x0765.*

    - UINT64 [SgxEpoch0](#)
  - Offset 0x0768 - SgxEpoch0 SgxEpoch0 default values.*

    - UINT64 [SgxEpoch1](#)
  - Offset 0x0770 - SgxEpoch1 SgxEpoch1 default values.*

    - UINT8 [MeUnconfigOnRtcClear](#)
  - Offset 0x0778 - Enable/Disable ME Unconfig on RTC clear Enable(Default): Enable ME Unconfig On Rtc Clear, Disable: Disable ME Unconfig On Rtc Clear \$EN\_DIS.*

    - UINT8 [MeUnconfigsValid](#)
  - Offset 0x0779 - Check if MeUnconfigOnRtcClear is valid The MeUnconfigOnRtcClear item could be not valid due to CMOS is clear.*

    - UINT8 [IsIVrCmd](#)
  - Offset 0x077A - Activates VR mailbox command for Intersil VR C-state issues.*

    - UINT8 [ReservedFspUpd](#) [5]
  - Offset 0x077B.*
-

### 8.6.1 Detailed Description

Fsp S Configuration.

Definition at line 88 of file FspUpd.h.

### 8.6.2 Member Data Documentation

#### 8.6.2.1 UINT16 FSP\_S\_CONFIG::AcLoadline[5]

Offset 0x0298 - AcLoadline PCODE MMIO Mailbox: AcLoadline in 1/100 mOhms (ie.

1250 = 12.50 mOhm); Range is 0-6249. **Intel Recommended Defaults vary by domain and SKU.**

Definition at line 698 of file FspUpd.h.

#### 8.6.2.2 UINT8 FSP\_S\_CONFIG::AcousticNoiseMitigation

Offset 0x0278 - Acoustic Noise Mitigation feature Enable or Disable Acoustic Noise Mitigation feature.

**0: Disabled**; 1: Enabled \$EN\_DIS

Definition at line 643 of file FspUpd.h.

#### 8.6.2.3 UINT8 FSP\_S\_CONFIG::AmtEnabled

Offset 0x0153 - AMT Switch Enable/Disable.

0: Disable, 1: enable, Enable or disable AMT functionality. \$EN\_DIS

Definition at line 410 of file FspUpd.h.

#### 8.6.2.4 UINT8 FSP\_S\_CONFIG::AmtSolEnabled

Offset 0x015C - SOL Switch Enable/Disable.

0: Disable, 1: enable, Serial Over Lan enable/disable state by Mebx \$EN\_DIS

Definition at line 453 of file FspUpd.h.

#### 8.6.2.5 UINT8 FSP\_S\_CONFIG::AsfEnabled

Offset 0x0155 - ASF Switch Enable/Disable.

0: Disable, 1: enable, Enable or disable ASF functionality. \$EN\_DIS

Definition at line 422 of file FspUpd.h.

#### 8.6.2.6 UINT16 FSP\_S\_CONFIG::DcLoadline[5]

Offset 0x02A2 - DcLoadline PCODE MMIO Mailbox: DcLoadline in 1/100 mOhms (ie.

1250 = 12.50 mOhm); Range is 0-6249. **Intel Recommended Defaults vary by domain and SKU.**

Definition at line 704 of file FspUpd.h.

#### 8.6.2.7 UINT8 FSP\_S\_CONFIG::DelayUsbPdoProgramming

Offset 0x00FC - Delay USB PDO Programming Enable/disable delay of PDO programming for USB from PEI phase to DXE phase.

---

0: disable, 1: enable \$EN\_DIS

Definition at line 373 of file FspsUpd.h.

#### 8.6.2.8 UINT32 FSP\_S\_CONFIG::DevIntConfigPtr

Offset 0x0070 - Address of PCH\_DEVICE\_INTERRUPT\_CONFIG table.

The address of the table of PCH\_DEVICE\_INTERRUPT\_CONFIG.

Definition at line 251 of file FspsUpd.h.

#### 8.6.2.9 UINT8 FSP\_S\_CONFIG::DmiSuggestedSetting

Offset 0x06E9 - DMI Thermal Sensor Suggested Setting DMT thermal sensor suggested representative values.

\$EN\_DIS

Definition at line 1854 of file FspsUpd.h.

#### 8.6.2.10 UINT8 FSP\_S\_CONFIG::Early8254ClockGatingEnable

Offset 0x071F - Enable 8254 Static Clock Gating in early POST time Set 8254CGE=1 is required for C11 support.

However, set 8254CGE=1 in POST time might fail to boot legacy OS which using 8254 timer. Make sure it won't break legacy OS boot before enabling this. \$EN\_DIS

Definition at line 1993 of file FspsUpd.h.

#### 8.6.2.11 UINT8 FSP\_S\_CONFIG::EcCmdLock

Offset 0x072A - EcCmdLock EcCmdLock default values.

Locks Ephemeral Authorization Value sent previously

Definition at line 2042 of file FspsUpd.h.

#### 8.6.2.12 UINT8 FSP\_S\_CONFIG::EcCmdProvisionEav

Offset 0x0729 - EcCmdProvisionEav Ephemeral Authorization Value default values.

Provisions an ephemeral shared secret to the EC

Definition at line 2037 of file FspsUpd.h.

#### 8.6.2.13 UINT8 FSP\_S\_CONFIG::EnableTcoTimer

Offset 0x0728 - Enable TCO timer.

When FALSE, it disables PCH ACPI timer, and stops TCO timer. NOTE: This will have huge power impact when it's enabled. If TCO timer is disabled, uCode ACPI timer emulation must be enabled, and WDAT table must not be exposed to the OS. \$EN\_DIS

Definition at line 2032 of file FspsUpd.h.

#### 8.6.2.14 UINT8 FSP\_S\_CONFIG::EsataSpeedLimit

Offset 0x065E - PCH Sata eSATA Speed Limit When enabled, BIOS will configure the PxSCTL.SPD to 2 to limit the eSATA port speed.

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\$EN\_DIS

Definition at line 1571 of file FspsUpd.h.

#### 8.6.2.15 UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableGt

Offset 0x02DF - Disable Fast Slew Rate for Deep Package C States for VR GT domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False;** 1: True \$EN\_DIS

Definition at line 743 of file FspsUpd.h.

#### 8.6.2.16 UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableIa

Offset 0x0279 - Disable Fast Slew Rate for Deep Package C States for VR IA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False;** 1: True \$EN\_DIS

Definition at line 650 of file FspsUpd.h.

#### 8.6.2.17 UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableSa

Offset 0x02E0 - Disable Fast Slew Rate for Deep Package C States for VR SA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False;** 1: True \$EN\_DIS

Definition at line 750 of file FspsUpd.h.

#### 8.6.2.18 UINT8 FSP\_S\_CONFIG::FwProgress

Offset 0x0157 - PET Progress Enable/Disable.

0: Disable, 1: enable, Enable/Disable PET Events Progress to receive PET Events. \$EN\_DIS

Definition at line 435 of file FspsUpd.h.

#### 8.6.2.19 UINT8 FSP\_S\_CONFIG::GpioIrqRoute

Offset 0x0087 - Select GPIO IRQ Route GPIO IRQ Select.

The valid value is 14 or 15.

Definition at line 270 of file FspsUpd.h.

#### 8.6.2.20 UINT8 FSP\_S\_CONFIG::Heci3Enabled

Offset 0x0149 - HECI3 state The HECI3 state from Mbp for reference in S3 path or when MbpHob is not installed.

0: disable, 1: enable \$EN\_DIS

Definition at line 400 of file FspsUpd.h.

#### 8.6.2.21 UINT8 FSP\_S\_CONFIG::HybridStorageMode

Offset 0x0722 - Hybrid Storage Mode Enables support for Hybrid storage devices.

0: Disabled; 1: Dynamic Configuration. Default is 0: Disabled \$EN\_DIS

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Definition at line 2012 of file FspsUpd.h.

#### 8.6.2.22 UINT16 FSP\_S\_CONFIG::IccMax[5]

Offset 0x02CA - Icc Max limit PCODE MMIO Mailbox: VR Icc Max limit.

0-255A in 1/4 A units. 400 = 100A

Definition at line 727 of file FspsUpd.h.

#### 8.6.2.23 UINT8 FSP\_S\_CONFIG::ImonOffset[5]

Offset 0x025D - Imon offset correction PCODE MMIO Mailbox: Imon offset correction.

Value is a 2's complement signed integer. Units 1/1000, Range 0-63999. For an offset = 12.580, use 12580. **0: Auto**

Definition at line 601 of file FspsUpd.h.

#### 8.6.2.24 UINT8 FSP\_S\_CONFIG::ImonSlope[5]

Offset 0x0258 - Imon slope correction PCODE MMIO Mailbox: Imon slope correction.

Specified in 1/100 increment values. Range is 0-200. 125 = 1.25. **0: Auto**. For all VR Indexes

Definition at line 595 of file FspsUpd.h.

#### 8.6.2.25 UINT8 FSP\_S\_CONFIG::IsIVrCmd

Offset 0x077A - Activates VR mailbox command for Intersil VR C-state issues.

Intersil VR mailbox command. **0 - no mailbox command sent**. 1 - VR mailbox command sent for IA/GT rails only. 2 - VR mailbox command sent for IA/GT/SA rails.

Definition at line 2105 of file FspsUpd.h.

#### 8.6.2.26 UINT8 FSP\_S\_CONFIG::ManageabilityMode

Offset 0x0156 - Manageability Mode set by Mebx Enable/Disable.

0: Disable, 1: enable, Enable or disable Manageability Mode. \$EN\_DIS

Definition at line 428 of file FspsUpd.h.

#### 8.6.2.27 UINT8 FSP\_S\_CONFIG::MeUnconfigsValid

Offset 0x0779 - Check if MeUnconfigOnRtcClear is valid The MeUnconfigOnRtcClear item could be not valid due to CMOS is clear.

\$EN\_DIS

Definition at line 2099 of file FspsUpd.h.

#### 8.6.2.28 UINT64 FSP\_S\_CONFIG::MicrocodePatchAddress

Offset 0x02F0 - MicrocodePatchAddress Pointer to microcode patch that is suitable for this processor.

0:Disable, 1:Enable

Definition at line 785 of file FspsUpd.h.

**8.6.2.29   UINT8 FSP\_S\_CONFIG::NumOfDevIntConfig**

Offset 0x006F - Number of DevIntConfig Entry Number of Device Interrupt Configuration Entry.

If this is not zero, the DevIntConfigPtr must not be NULL.

Definition at line 246 of file FspsUpd.h.

**8.6.2.30   UINT8 FSP\_S\_CONFIG::PchCio2Enable**

Offset 0x0030 - Enable CIO2 Controller Enable/disable SKYCAM CIO2 Controller.

\$EN\_DIS

Definition at line 137 of file FspsUpd.h.

**8.6.2.31   UINT8 FSP\_S\_CONFIG::PchCrid**

Offset 0x0365 - PCH Compatibility Revision ID This member describes whether or not the CRID feature of PCH should be enabled.

\$EN\_DIS

Definition at line 1202 of file FspsUpd.h.

**8.6.2.32   UINT8 FSP\_S\_CONFIG::PchDisableComplianceMode**

Offset 0x0704 - Disable XHCI Compliance Mode This policy will disable XHCI compliance mode on all ports.

Complicance Mode should be default enabled. \$EN\_DIS

Definition at line 1975 of file FspsUpd.h.

**8.6.2.33   UINT8 FSP\_S\_CONFIG::PchDmiAspm**

Offset 0x0316 - Enable DMI ASPM ASPM on PCH side of the DMI Link.

\$EN\_DIS

Definition at line 931 of file FspsUpd.h.

**8.6.2.34   UINT8 FSP\_S\_CONFIG::PchDmiTsawEn**

Offset 0x06E8 - DMI Thermal Sensor Autonomous Width Enable DMI Thermal Sensor Autonomous Width Enable.

\$EN\_DIS

Definition at line 1848 of file FspsUpd.h.

**8.6.2.35   UINT8 FSP\_S\_CONFIG::PchHdaDspEnable**

Offset 0x002E - Enable HD Audio DSP Enable/disable HD Audio DSP feature.

\$EN\_DIS

Definition at line 121 of file FspsUpd.h.

**8.6.2.36   UINT8 FSP\_S\_CONFIG::PchHdaDspEndpointBluetooth**

Offset 0x033F - DSP Bluetooth enablement 0: Disable; 1: Enable.

---

\$EN\_DIS

Definition at line 1013 of file FspsUpd.h.

#### 8.6.2.37 UINT8 FSP\_S\_CONFIG::PchHdaDspEndpointI2s

Offset 0x0348 - DSP I2S enablement 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1033 of file FspsUpd.h.

#### 8.6.2.38 UINT32 FSP\_S\_CONFIG::PchHdaDspFeatureMask

Offset 0x0340 - Bitmask of supported DSP features [BIT0] - WoV; [BIT1] - BT Sideband; [BIT2] - Codec VAD; [BIT5] - BT Intel HFP; [BIT6].

- BT Intel A2DP; [BIT7] - DSP based speech pre-processing disabled; [BIT8] - 0: Intel WoV, 1: Windows Voice Activation.

Definition at line 1020 of file FspsUpd.h.

#### 8.6.2.39 UINT8 FSP\_S\_CONFIG::PchHdaDspUaaCompliance

Offset 0x033C - Universal Audio Architecture compliance for DSP enabled system 0: Not-UAA Compliant (Intel SST driver supported only), 1: UAA Compliant (HDA Inbox driver or SST driver supported).

\$EN\_DIS

Definition at line 996 of file FspsUpd.h.

#### 8.6.2.40 UINT8 FSP\_S\_CONFIG::PchHdaEnable

Offset 0x002D - Enable Intel HD Audio (Azalia) Enable/disable Azalia controller.

\$EN\_DIS

Definition at line 115 of file FspsUpd.h.

#### 8.6.2.41 UINT8 FSP\_S\_CONFIG::PchHdaDispCodecDisconnect

Offset 0x033D - iDisplay Audio Codec disconnection 0: Not disconnected, enumerable, 1: Disconnected SDI, not enumerable.

\$EN\_DIS

Definition at line 1002 of file FspsUpd.h.

#### 8.6.2.42 UINT8 FSP\_S\_CONFIG::PchHdaIoBufferOwnership

Offset 0x002F - Select HDAudio IoBuffer Ownership Indicates the ownership of the I/O buffer between Intel HD Audio link vs I2S0 / I2S1 port.

0: Intel HD-Audio link owns all the I/O buffers. 1: Intel HD-Audio link owns 4 of the I/O buffers for 1 HD-Audio codec connection, and I2S1 port owns 4 of the I/O buffers for 1 I2S codec connection. 2: Reserved. 3: I2S0 and I2S1 ports own all the I/O buffers. 0:HD-A Link, 1:Shared HD-A Link and I2S Port, 3:I2S Ports

Definition at line 131 of file FspsUpd.h.

**8.6.2.43   UINT8 FSP\_S\_CONFIG::PchHdaPme**

Offset 0x0336 - Enable Pme Enable Azalia wake-on-ring.

\$EN\_DIS

Definition at line 964 of file FspsUpd.h.

**8.6.2.44   UINT8 FSP\_S\_CONFIG::PchIoApicBdfValid**

Offset 0x0349 - Enable PCH Io Apic Set to 1 if BDF value is valid.

\$EN\_DIS

Definition at line 1039 of file FspsUpd.h.

**8.6.2.45   UINT8 FSP\_S\_CONFIG::PchIoApicBusNumber**

Offset 0x034A - PCH Io Apic Bus Number Bus/Device/Function used as Requestor / Completer ID.

Default is 0xF0.

Definition at line 1044 of file FspsUpd.h.

**8.6.2.46   UINT8 FSP\_S\_CONFIG::PchIoApicDeviceNumber**

Offset 0x034B - PCH Io Apic Device Number Bus/Device/Function used as Requestor / Completer ID.

Default is 0x1F.

Definition at line 1049 of file FspsUpd.h.

**8.6.2.47   UINT8 FSP\_S\_CONFIG::PchIoApicEntry24\_119**

Offset 0x034D - Enable PCH Io Apic Entry 24-119 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1060 of file FspsUpd.h.

**8.6.2.48   UINT8 FSP\_S\_CONFIG::PchIoApicFunctionNumber**

Offset 0x034C - PCH Io Apic Function Number Bus/Device/Function used as Requestor / Completer ID.

Default is 0x00.

Definition at line 1054 of file FspsUpd.h.

**8.6.2.49   UINT8 FSP\_S\_CONFIG::PchIoApicId**

Offset 0x034E - PCH Io Apic ID This member determines IOAPIC ID.

Default is 0x02.

Definition at line 1065 of file FspsUpd.h.

**8.6.2.50   UINT8 FSP\_S\_CONFIG::PchIoApicRangeSelect**

Offset 0x034F - PCH Io Apic Range Select Define address bits 19:12 for the IOxAPIC range.

Default is 0.

---



Definition at line 1070 of file FspsUpd.h.

#### 8.6.2.51 UINT8 FSP\_S\_CONFIG::PchIshEnable

Offset 0x0034 - Enable PCH ISH Controller Enable/disable ISH Controller.

\$EN\_DIS

Definition at line 161 of file FspsUpd.h.

#### 8.6.2.52 UINT8 FSP\_S\_CONFIG::PchIshGp0GpioAssign

Offset 0x0356 - Enable PCH ISH GP\_0 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1112 of file FspsUpd.h.

#### 8.6.2.53 UINT8 FSP\_S\_CONFIG::PchIshGp1GpioAssign

Offset 0x0357 - Enable PCH ISH GP\_1 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1118 of file FspsUpd.h.

#### 8.6.2.54 UINT8 FSP\_S\_CONFIG::PchIshGp2GpioAssign

Offset 0x0358 - Enable PCH ISH GP\_2 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1124 of file FspsUpd.h.

#### 8.6.2.55 UINT8 FSP\_S\_CONFIG::PchIshGp3GpioAssign

Offset 0x0359 - Enable PCH ISH GP\_3 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1130 of file FspsUpd.h.

#### 8.6.2.56 UINT8 FSP\_S\_CONFIG::PchIshGp4GpioAssign

Offset 0x035A - Enable PCH ISH GP\_4 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1136 of file FspsUpd.h.

#### 8.6.2.57 UINT8 FSP\_S\_CONFIG::PchIshGp5GpioAssign

Offset 0x035B - Enable PCH ISH GP\_5 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1142 of file FspsUpd.h.

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**8.6.2.58    UINT8 FSP\_S\_CONFIG::PchIshGp6GpioAssign**

Offset 0x035C - Enable PCH ISH GP\_6 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1148 of file FspsUpd.h.

**8.6.2.59    UINT8 FSP\_S\_CONFIG::PchIshGp7GpioAssign**

Offset 0x035D - Enable PCH ISH GP\_7 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1154 of file FspsUpd.h.

**8.6.2.60    UINT8 FSP\_S\_CONFIG::PchIshI2c0GpioAssign**

Offset 0x0353 - Enable PCH ISH I2C0 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1094 of file FspsUpd.h.

**8.6.2.61    UINT8 FSP\_S\_CONFIG::PchIshI2c1GpioAssign**

Offset 0x0354 - Enable PCH ISH I2C1 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1100 of file FspsUpd.h.

**8.6.2.62    UINT8 FSP\_S\_CONFIG::PchIshI2c2GpioAssign**

Offset 0x0355 - Enable PCH ISH I2C2 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1106 of file FspsUpd.h.

**8.6.2.63    UINT8 FSP\_S\_CONFIG::PchIshPdtUnlock**

Offset 0x035E - PCH ISH PDT Unlock Msg 0: False; 1: True.

\$EN\_DIS

Definition at line 1160 of file FspsUpd.h.

**8.6.2.64    UINT8 FSP\_S\_CONFIG::PchIshSpiGpioAssign**

Offset 0x0350 - Enable PCH ISH SPI GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1076 of file FspsUpd.h.

**8.6.2.65    UINT8 FSP\_S\_CONFIG::PchIshUart0GpioAssign**

Offset 0x0351 - Enable PCH ISH UART0 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

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Definition at line 1082 of file FspsUpd.h.

#### 8.6.2.66 UINT8 FSP\_S\_CONFIG::PchIshUart1GpioAssign

Offset 0x0352 - Enable PCH ISH UART1 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1088 of file FspsUpd.h.

#### 8.6.2.67 UINT8 FSP\_S\_CONFIG::PchLanClkReqSupported

Offset 0x0361 - Indicate whether dedicated CLKREQ# is supported 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1178 of file FspsUpd.h.

#### 8.6.2.68 UINT8 FSP\_S\_CONFIG::PchLanEnable

Offset 0x00FB - Enable LAN Enable/disable LAN controller.

\$EN\_DIS

Definition at line 366 of file FspsUpd.h.

#### 8.6.2.69 UINT8 FSP\_S\_CONFIG::PchLanK10ffEnable

Offset 0x0360 - Enable PCH Lan use CLKREQ for GbE power management 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1172 of file FspsUpd.h.

#### 8.6.2.70 UINT8 FSP\_S\_CONFIG::PchLanLtrEnable

Offset 0x035F - Enable PCH Lan LTR capability of PCH internal LAN 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line 1166 of file FspsUpd.h.

#### 8.6.2.71 UINT8 FSP\_S\_CONFIG::PchLockDownBiosLock

Offset 0x0363 - Enable LOCKDOWN BIOS LOCK Enable the BIOS Lock feature and set EISS bit (D31:F5:RegD↔Ch[5]) for the BIOS region protection.

\$EN\_DIS

Definition at line 1190 of file FspsUpd.h.

#### 8.6.2.72 UINT8 FSP\_S\_CONFIG::PchLockDownSpiEiss

Offset 0x0364 - Enable LOCKDOWN SPI Eiss Enable InSMM.STS (EISS) in SPI.

\$EN\_DIS

Definition at line 1196 of file FspsUpd.h.

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#### 8.6.2.73 UINT8 FSP\_S\_CONFIG::PchMemoryThrottlingEnable

Offset 0x06FB - Enable Memory Thermal Throttling Enable Memory Thermal Throttling.

\$EN\_DIS

Definition at line 1948 of file FspUpd.h.

#### 8.6.2.74 UINT32 FSP\_S\_CONFIG::PchPcieDeviceOverrideTablePtr

Offset 0x0724 - Pch PCIE device override table pointer The PCIE device table is being used to override PCIE device ASPM settings.

This is a pointer points to a 32bit address. And it's only used in PostMem phase. Please refer to PCH\_PCIE\_DEVICE\_OVERRIDE structure for the table. Last entry VendorId must be 0.

Definition at line 2024 of file FspUpd.h.

#### 8.6.2.75 UINT8 FSP\_S\_CONFIG::PchPmCapsuleResetType

Offset 0x0655 - PCH Pm Capsule Reset Type Deprecated: Determines type of reset issued during UpdateCapsule().

Always Warm reset. \$EN\_DIS

Definition at line 1518 of file FspUpd.h.

#### 8.6.2.76 UINT8 FSP\_S\_CONFIG::PchPmDeepSxPol

Offset 0x0645 - PCH Pm Deep Sx Pol Deep Sx Policy.

\$EN\_DIS

Definition at line 1459 of file FspUpd.h.

#### 8.6.2.77 UINT8 FSP\_S\_CONFIG::PchPmDisableDsxAcPresentPulldown

Offset 0x0654 - PCH Pm Disable Dsx Ac Present Pulldown When Disable, PCH will internal pull down AC\_PRESENT in deep SX and during G3 exit.

\$EN\_DIS

Definition at line 1512 of file FspUpd.h.

#### 8.6.2.78 UINT8 FSP\_S\_CONFIG::PchPmDisableNativePowerButton

Offset 0x0656 - PCH Pm Disable Native Power Button Power button native mode disable.

\$EN\_DIS

Definition at line 1524 of file FspUpd.h.

#### 8.6.2.79 UINT8 FSP\_S\_CONFIG::PchPmLanWakeFromDeepSx

Offset 0x0644 - PCH Pm Lan Wake From DeepSx Determine if enable LAN to wake from deep Sx.

\$EN\_DIS

Definition at line 1453 of file FspUpd.h.

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**8.6.2.80   UINT8 FSP\_S\_CONFIG::PchPmLpcClockRun**

Offset 0x0650 - PCH Pm Lpc Clock Run This member describes whether or not the LPC ClockRun feature of PCH should be enabled.

\$EN\_DIS

Definition at line 1489 of file FspsUpd.h.

**8.6.2.81   UINT8 FSP\_S\_CONFIG::PchPmMeWakeSts**

Offset 0x0658 - PCH Pm ME\_WAKE\_STS Clear the ME\_WAKE\_STS bit in the Power and Reset Status (PRSTS) register.

\$EN\_DIS

Definition at line 1536 of file FspsUpd.h.

**8.6.2.82   UINT8 FSP\_S\_CONFIG::PchPmPcieWakeFromDeepSx**

Offset 0x0641 - PCH Pm Pcie Wake From DeepSx Determine if enable PCIe to wake from deep Sx.

\$EN\_DIS

Definition at line 1434 of file FspsUpd.h.

**8.6.2.83   UINT8 FSP\_S\_CONFIG::PchPmPmeB0S5Dis**

Offset 0x0639 - PCH Pm PME\_B0\_S5\_DIS When cleared (default), wake events from PME\_B0\_STS are allowed in S5 if PME\_B0\_EN = 1.

\$EN\_DIS

Definition at line 1412 of file FspsUpd.h.

**8.6.2.84   UINT8 FSP\_S\_CONFIG::PchPmPwrBtnOverridePeriod**

Offset 0x0653 - PCH Pm Pwr Btn Override Period PCH power button override period.

000b-4s, 001b-6s, 010b-8s, 011b-10s, 100b-12s, 101b-14s.

Definition at line 1506 of file FspsUpd.h.

**8.6.2.85   UINT8 FSP\_S\_CONFIG::PchPmPwrCycDur**

Offset 0x065A - PCH Pm Reset Power Cycle Duration Could be customized in the unit of second.

Please refer to EDS for all support settings. 0 is default, 1 is 1 second, 2 is 2 seconds, ...

Definition at line 1548 of file FspsUpd.h.

**8.6.2.86   UINT8 FSP\_S\_CONFIG::PchPmSlpAMinAssert**

Offset 0x0649 - PCH Pm Slp A Min Assert SLP\_A Minimum Assertion Width Policy.

Default is PchSlpA2s.

Definition at line 1479 of file FspsUpd.h.

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**8.6.2.87 UINT8 FSP\_S\_CONFIG::PchPmSlpLanLowDc**

Offset 0x0652 - PCH Pm Slp Lan Low Dc Enable/Disable SLP\_LAN# Low on DC Power.

\$EN\_DIS

Definition at line 1501 of file FspsUpd.h.

**8.6.2.88 UINT8 FSP\_S\_CONFIG::PchPmSlpS0Enable**

Offset 0x0657 - PCH Pm Slp S0 Enable Indicates whether SLP\_S0# is to be asserted when PCH reaches idle state.

\$EN\_DIS

Definition at line 1530 of file FspsUpd.h.

**8.6.2.89 UINT8 FSP\_S\_CONFIG::PchPmSlpS0VmEnable**

Offset 0x063A - PCH Pm Slp S0 Voltage Margining Enable Indicates platform has support for VCCPrim\_Core Voltage Margining in SLP\_S0# asserted state.

\$EN\_DIS

Definition at line 1418 of file FspsUpd.h.

**8.6.2.90 UINT8 FSP\_S\_CONFIG::PchPmSlpS3MinAssert**

Offset 0x0646 - PCH Pm Slp S3 Min Assert SLP\_S3 Minimum Assertion Width Policy.

Default is PchSlpS350ms.

Definition at line 1464 of file FspsUpd.h.

**8.6.2.91 UINT8 FSP\_S\_CONFIG::PchPmSlpS4MinAssert**

Offset 0x0647 - PCH Pm Slp S4 Min Assert SLP\_S4 Minimum Assertion Width Policy.

Default is PchSlpS44s.

Definition at line 1469 of file FspsUpd.h.

**8.6.2.92 UINT8 FSP\_S\_CONFIG::PchPmSlpStrchSusUp**

Offset 0x0651 - PCH Pm Slp Strch Sus Up Enable SLP\_X Stretching After SUS Well Power Up.

\$EN\_DIS

Definition at line 1495 of file FspsUpd.h.

**8.6.2.93 UINT8 FSP\_S\_CONFIG::PchPmSlpSusMinAssert**

Offset 0x0648 - PCH Pm Slp Sus Min Assert SLP\_SUS Minimum Assertion Width Policy.

Default is PchSlpSus4s.

Definition at line 1474 of file FspsUpd.h.

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**8.6.2.94   UINT8 FSP\_S\_CONFIG::PchPmWolEnableOverride**

Offset 0x0640 - PCH Pm Wol Enable Override Corresponds to the WOL Enable Override bit in the General PM Configuration B (GEN\_PMCON\_B) register.

\$EN\_DIS

Definition at line 1428 of file FspUpd.h.

**8.6.2.95   UINT8 FSP\_S\_CONFIG::PchPmWolOvrWkSts**

Offset 0x0659 - PCH Pm WOL\_OVR\_WK\_STS Clear the WOL\_OVR\_WK\_STS bit in the Power and Reset Status (PRSTS) register.

\$EN\_DIS

Definition at line 1542 of file FspUpd.h.

**8.6.2.96   UINT8 FSP\_S\_CONFIG::PchPmWoWlanDeepSxEnable**

Offset 0x0643 - PCH Pm WoW lan DeepSx Enable Determine if WLAN wake from DeepSx, corresponds to the DSX\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.

\$EN\_DIS

Definition at line 1447 of file FspUpd.h.

**8.6.2.97   UINT8 FSP\_S\_CONFIG::PchPmWoWlanEnable**

Offset 0x0642 - PCH Pm WoW lan Enable Determine if WLAN wake from Sx, corresponds to the HOST\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.

\$EN\_DIS

Definition at line 1440 of file FspUpd.h.

**8.6.2.98   UINT8 FSP\_S\_CONFIG::PchPort61hEnable**

Offset 0x065C - PCH Port 61h Config Enable/Disable Used for the emulation feature for Port61h read.

The port is trapped and the SMI handler will toggle bit4 according to the handler's internal state. \$EN\_DIS

Definition at line 1559 of file FspUpd.h.

**8.6.2.99   UINT8 FSP\_S\_CONFIG::PchPwrOptEnable**

Offset 0x0317 - Enable Power Optimizer Enable DMI Power Optimizer on PCH side.

\$EN\_DIS

Definition at line 937 of file FspUpd.h.

**8.6.2.100   UINT8 FSP\_S\_CONFIG::PchScsEmmcHs400DIIDataValid**

Offset 0x06C6 - Set HS400 Tuning Data Valid Set if HS400 Tuning Data Valid.

\$EN\_DIS

Definition at line 1720 of file FspUpd.h.

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**8.6.2.101    UINT8 FSP\_S\_CONFIG::PchScsEmmcHs400TuningRequired**

Offset 0x06C5 - Enable eMMC HS400 Training Determine if HS400 Training is required.

\$EN\_DIS

Definition at line 1714 of file FspsUpd.h.

**8.6.2.102    UINT8 FSP\_S\_CONFIG::PchSirqEnable**

Offset 0x06D8 - Enable Serial IRQ Determines if enable Serial IRQ.

\$EN\_DIS

Definition at line 1773 of file FspsUpd.h.

**8.6.2.103    UINT8 FSP\_S\_CONFIG::PchSirqMode**

Offset 0x06D9 - Serial IRQ Mode Select Serial IRQ Mode Select, 0: quiet mode, 1: continuous mode.

\$EN\_DIS

Definition at line 1779 of file FspsUpd.h.

**8.6.2.104    UINT8 FSP\_S\_CONFIG::PchSkyCamPortACtleEnable**

Offset 0x0303 - Enable SkyCam PortA Ctle Enable/disable PortA Ctle.

\$EN\_DIS

Definition at line 848 of file FspsUpd.h.

**8.6.2.105    UINT8 FSP\_S\_CONFIG::PchSkyCamPortATermOvrEnable**

Offset 0x02FB - Enable SkyCam PortA Termination override Enable/disable PortA Termination override.

\$EN\_DIS

Definition at line 800 of file FspsUpd.h.

**8.6.2.106    UINT8 FSP\_S\_CONFIG::PchSkyCamPortATrimEnable**

Offset 0x02FF - Enable SkyCam PortA Clk Trim Enable/disable PortA Clk Trim.

\$EN\_DIS

Definition at line 824 of file FspsUpd.h.

**8.6.2.107    UINT8 FSP\_S\_CONFIG::PchSkyCamPortBCtleEnable**

Offset 0x0304 - Enable SkyCam PortB Ctle Enable/disable PortB Ctle.

\$EN\_DIS

Definition at line 854 of file FspsUpd.h.

**8.6.2.108    UINT8 FSP\_S\_CONFIG::PchSkyCamPortBTermOvrEnable**

Offset 0x02FC - Enable SkyCam PortB Termination override Enable/disable PortB Termination override.

\$EN\_DIS

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Definition at line 806 of file FspsUpd.h.

#### 8.6.2.109 UINT8 FSP\_S\_CONFIG::PchSkyCamPortBTrimEnable

Offset 0x0300 - Enable SkyCam PortB Clk Trim Enable/disable PortB Clk Trim.

\$EN\_DIS

Definition at line 830 of file FspsUpd.h.

#### 8.6.2.110 UINT8 FSP\_S\_CONFIG::PchSkyCamPortCDClteEnable

Offset 0x0305 - Enable SkyCam PortCD Clte Enable/disable PortCD Clte.

\$EN\_DIS

Definition at line 860 of file FspsUpd.h.

#### 8.6.2.111 UINT8 FSP\_S\_CONFIG::PchSkyCamPortCTermOvrEnable

Offset 0x02FD - Enable SkyCam PortC Termination override Enable/disable PortC Termination override.

\$EN\_DIS

Definition at line 812 of file FspsUpd.h.

#### 8.6.2.112 UINT8 FSP\_S\_CONFIG::PchSkyCamPortCTrimEnable

Offset 0x0301 - Enable SkyCam PortC Clk Trim Enable/disable PortC Clk Trim.

\$EN\_DIS

Definition at line 836 of file FspsUpd.h.

#### 8.6.2.113 UINT8 FSP\_S\_CONFIG::PchSkyCamPortDTermOvrEnable

Offset 0x02FE - Enable SkyCam PortD Termination override Enable/disable PortD Termination override.

\$EN\_DIS

Definition at line 818 of file FspsUpd.h.

#### 8.6.2.114 UINT8 FSP\_S\_CONFIG::PchSkyCamPortDTrimEnable

Offset 0x0302 - Enable SkyCam PortD Clk Trim Enable/disable PortD Clk Trim.

\$EN\_DIS

Definition at line 842 of file FspsUpd.h.

#### 8.6.2.115 UINT16 FSP\_S\_CONFIG::PchSubSystemId

Offset 0x0368 - PCH Sub system ID Default Subsystem ID of the PCH devices.

Default is 0x7270.

Definition at line 1212 of file FspsUpd.h.

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**8.6.2.116    UINT16 FSP\_S\_CONFIG::PchSubSystemVendorId**

Offset 0x0366 - PCH Sub system vendor ID Default Subsystem Vendor ID of the PCH devices.

Default is 0x8086.

Definition at line 1207 of file FspUpd.h.

**8.6.2.117    UINT8 FSP\_S\_CONFIG::PchThermalDeviceEnable**

Offset 0x06DB - Enable Thermal Device Enable Thermal Device.

\$EN\_DIS

Definition at line 1790 of file FspUpd.h.

**8.6.2.118    UINT8 FSP\_S\_CONFIG::PchTsmicLock**

Offset 0x06E2 - Thermal Device SMI Enable This locks down SMI Enable on Alert Thermal Sensor Trip.

\$EN\_DIS

Definition at line 1811 of file FspUpd.h.

**8.6.2.119    UINT8 FSP\_S\_CONFIG::PchTTEnable**

Offset 0x06E3 - Enable The Thermal Throttle Enable the thermal throttle function.

\$EN\_DIS

Definition at line 1817 of file FspUpd.h.

**8.6.2.120    UINT8 FSP\_S\_CONFIG::PchTTLock**

Offset 0x06E5 - Thermal Throttle Lock Thermal Throttle Lock.

\$EN\_DIS

Definition at line 1830 of file FspUpd.h.

**8.6.2.121    UINT8 FSP\_S\_CONFIG::PchTTState13Enable**

Offset 0x06E4 - PMSync State 13 When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 will force at least T2 state.

\$EN\_DIS

Definition at line 1824 of file FspUpd.h.

**8.6.2.122    UINT8 FSP\_S\_CONFIG::PcieAllowNoLtrIccPllShutdown**

Offset 0x0634 - PCIE Allow No Ltr Icc PLL Shutdown Allows BIOS to control ICC PLL Shutdown by determining PCIe devices are LTR capable or leaving untouched.

\$EN\_DIS

Definition at line 1387 of file FspUpd.h.

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**8.6.2.123   UINT8 FSP\_S\_CONFIG::PcieComplianceTestMode**

Offset 0x0635 - PCIE Compliance Test Mode Compliance Test Mode shall be enabled when using Compliance Load Board.

\$EN\_DIS

Definition at line 1393 of file FspUpd.h.

**8.6.2.124   UINT8 FSP\_S\_CONFIG::PcieDisableRootPortClockGating**

Offset 0x0632 - PCIE Disable RootPort Clock Gating Describes whether the PCI Express Clock Gating for each root port is enabled by platform modules.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line 1374 of file FspUpd.h.

**8.6.2.125   UINT8 FSP\_S\_CONFIG::PcieEnablePeerMemoryWrite**

Offset 0x0633 - PCIE Enable Peer Memory Write This member describes whether Peer Memory Writes are enabled on the platform.

\$EN\_DIS

Definition at line 1380 of file FspUpd.h.

**8.6.2.126   UINT8 FSP\_S\_CONFIG::PcieEqPh3LaneParamCm[24]**

Offset 0x05F8 - PCIE Eq Ph3 Lane Param Cm PCH\_PCIE\_EQ\_LANE\_PARAM.

Coefficient C-1.

Definition at line 1352 of file FspUpd.h.

**8.6.2.127   UINT8 FSP\_S\_CONFIG::PcieEqPh3LaneParamCp[24]**

Offset 0x0610 - PCIE Eq Ph3 Lane Param Cp PCH\_PCIE\_EQ\_LANE\_PARAM.

Coefficient C+1.

Definition at line 1357 of file FspUpd.h.

**8.6.2.128   UINT8 FSP\_S\_CONFIG::PcieRpAspm[24]**

Offset 0x0598 - PCIE RP Aspm The ASPM configuration of the root port (see: PCH\_PCIE\_ASPM\_CONTROL).

Default is PchPcieAspmAutoConfig.

Definition at line 1331 of file FspUpd.h.

**8.6.2.129   UINT8 FSP\_S\_CONFIG::PcieRpClkReqNumber[24]**

Offset 0x012C - Configure CLKREQ Number Configure Root Port CLKREQ Number if CLKREQ is supported.

Each value in array can be between 0-6. One byte for each port, byte0 for port1, byte1 for port2, and so on.

Definition at line 389 of file FspUpd.h.

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**8.6.2.130   UINT8 FSP\_S\_CONFIG::PcieRpClkReqSupport[24]**

Offset 0x0114 - Enable PCIE RP CLKREQ Support Enable/disable PCIE Root Port CLKREQ support.

0: disable, 1: enable. One byte for each port, byte0 for port1, byte1 for port2, and so on.

Definition at line 383 of file FspsUpd.h.

**8.6.2.131   UINT8 FSP\_S\_CONFIG::PcieRpClkSrcNumber[24]**

Offset 0x015D - Configure CLKSRC Number Configure Root Port CLKSRC Number.

Each value in array can be between 0-6 for valid clock numbers or 0x1F for an invalid number. One byte for each port, byte0 for port1, byte1 for port2, and so on.

Definition at line 460 of file FspsUpd.h.

**8.6.2.132   UINT8 FSP\_S\_CONFIG::PcieRpCompletionTimeout[24]**

Offset 0x0520 - PCIE RP Completion Timeout The root port completion timeout(see: PCH\_PCIE\_COMPLETION\_TIMEOUT).

Default is PchPcieCompletionTO\_Default.

Definition at line 1319 of file FspsUpd.h.

**8.6.2.133   UINT32 FSP\_S\_CONFIG::PcieRpDeviceResetPad[24]**

Offset 0x0538 - PCIE RP Device Reset Pad The PCH pin assigned to device PERST# signal if available, zero otherwise.

See also DeviceResetPadActiveHigh.

Definition at line 1325 of file FspsUpd.h.

**8.6.2.134   UINT8 FSP\_S\_CONFIG::PcieRpFunctionSwap**

Offset 0x0638 - PCIE Rp Function Swap Allows BIOS to use root port function number swapping when root port of function 0 is disabled.

\$EN\_DIS

Definition at line 1406 of file FspsUpd.h.

**8.6.2.135   UINT8 FSP\_S\_CONFIG::PcieRpGen3EqPh3Method[24]**

Offset 0x04F0 - PCIE RP Gen3 Equalization Phase Method PCIe Gen3 Eq Ph3 Method (see PCH\_PCIE\_EQ\_METHOD).

0: Default; 2: Software Search; 4: Fixed Coefficients.

Definition at line 1309 of file FspsUpd.h.

**8.6.2.136   UINT8 FSP\_S\_CONFIG::PcieRpL1Substates[24]**

Offset 0x05B0 - PCIE RP L1 Substates The L1 Substates configuration of the root port (see: PCH\_PCIE\_L1SUBSTATES\_CONTROL).

Default is PchPcieL1SubstatesL1\_1\_2.

Definition at line 1337 of file FspsUpd.h.

**8.6.2.137   UINT8 FSP\_S\_CONFIG::PcieRpPcieSpeed[24]**

Offset 0x04D8 - PCIE RP Pcie Speed Determines each PCIE Port speed capability.

0: Auto; 1: Gen1; 2: Gen2; 3: Gen3 (see: PCH\_PCIE\_SPEED).

Definition at line 1303 of file FspsUpd.h.

**8.6.2.138   UINT8 FSP\_S\_CONFIG::PcieRpPhysicalSlotNumber[24]**

Offset 0x0508 - PCIE RP Physical Slot Number Indicates the slot number for the root port.

Default is the value as root port index.

Definition at line 1314 of file FspsUpd.h.

**8.6.2.139   UINT8 FSP\_S\_CONFIG::PcieSwEqCoeffListCm[5]**

Offset 0x0628 - PCIE Sw Eq CoeffList Cm PCH\_PCIE\_EQ\_PARAM.

Coefficient C-1.

Definition at line 1362 of file FspsUpd.h.

**8.6.2.140   UINT8 FSP\_S\_CONFIG::PcieSwEqCoeffListCp[5]**

Offset 0x062D - PCIE Sw Eq CoeffList Cp PCH\_PCIE\_EQ\_PARAM.

Coefficient C+1.

Definition at line 1367 of file FspsUpd.h.

**8.6.2.141   UINT8 FSP\_S\_CONFIG::PortUsb20Enable[16]**

Offset 0x0052 - Enable USB2 ports Enable/disable per USB2 ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line 218 of file FspsUpd.h.

**8.6.2.142   UINT8 FSP\_S\_CONFIG::PortUsb30Enable[10]**

Offset 0x0062 - Enable USB3 ports Enable/disable per USB3 ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line 224 of file FspsUpd.h.

**8.6.2.143   UINT16 FSP\_S\_CONFIG::Psi1Threshold[5]**

Offset 0x02AC - Power State 1 Threshold current PCODE MMIO Mailbox: Power State 1 current cutoff in 1/4 Amp increments.

Range is 0-128A. Default Value = 20A.

Definition at line 710 of file FspsUpd.h.

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**8.6.2.144**    **UINT16 FSP\_S\_CONFIG::Psi2Threshold[5]**

Offset 0x02B6 - Power State 2 Threshold current PCODE MMIO Mailbox: Power State 2 current cutoff in 1/4 Amp increments.

Range is 0-128A. Default Value = 5A.

Definition at line 716 of file FspsUpd.h.

**8.6.2.145**    **UINT8 FSP\_S\_CONFIG::Psi3Enable[5]**

Offset 0x024E - Power State 3 enable/disable PCODE MMIO Mailbox: Power State 3 enable/disable; 0: Disable; **1: Enable**.

For all VR Indexes

Definition at line 583 of file FspsUpd.h.

**8.6.2.146**    **UINT16 FSP\_S\_CONFIG::Psi3Threshold[5]**

Offset 0x02C0 - Power State 3 Threshold current PCODE MMIO Mailbox: Power State 3 current cutoff in 1/4 Amp increments.

Range is 0-128A. Default Value = 1A.

Definition at line 722 of file FspsUpd.h.

**8.6.2.147**    **UINT8 FSP\_S\_CONFIG::PsysOffset**

Offset 0x0277 - Platform Psys offset correction PCODE MMIO Mailbox: Platform Psys offset correction.

**0 - Auto** Units 1/4, Range 0-255. Value of 100 =  $100/4 = 25$  offset

Definition at line 637 of file FspsUpd.h.

**8.6.2.148**    **UINT8 FSP\_S\_CONFIG::PsysSlope**

Offset 0x0276 - Platform Psys slope correction PCODE MMIO Mailbox: Platform Psys slope correction.

**0 - Auto** Specified in 1/100 increment values. Range is 0-200. 125 = 1.25

Definition at line 631 of file FspsUpd.h.

**8.6.2.149**    **UINT8 FSP\_S\_CONFIG::PxRcConfig[8]**

Offset 0x007F - PIRQx to IRQx Map Config PIRQx to IRQx mapping.

The valid value is 0x00 to 0x0F for each. First byte is for PIRQA, second byte is for PIRQB, and so on. The setting is only available in Legacy 8259 PCI mode.

Definition at line 265 of file FspsUpd.h.

**8.6.2.150**    **UINT8 FSP\_S\_CONFIG::SataEnable**

Offset 0x0091 - Enable SATA Enable/disable SATA controller.

\$EN\_DIS

Definition at line 306 of file FspsUpd.h.

**8.6.2.151   UINT8 FSP\_S\_CONFIG::SataMode**

Offset 0x0092 - SATA Mode Select SATA controller working mode.

0:AHCI, 1:RAID

Definition at line 312 of file FspsUpd.h.

**8.6.2.152   UINT8 FSP\_S\_CONFIG::SataP0TDispFinit**

Offset 0x06F7 - Port 0 Alternate Fast Init Tdispatch Port 0 Alternate Fast Init Tdispatch.

\$EN\_DIS

Definition at line 1925 of file FspsUpd.h.

**8.6.2.153   UINT8 FSP\_S\_CONFIG::SataP1TDispFinit**

Offset 0x06F9 - Port 1 Alternate Fast Init Tdispatch Port 1 Alternate Fast Init Tdispatch.

\$EN\_DIS

Definition at line 1936 of file FspsUpd.h.

**8.6.2.154   UINT8 FSP\_S\_CONFIG::SataPortsDevSlp[8]**

Offset 0x004A - Enable SATA DEVSLP Feature Enable/disable SATA DEVSLP per port.

0 is disable, 1 is enable. One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line 212 of file FspsUpd.h.

**8.6.2.155   UINT8 FSP\_S\_CONFIG::SataPortsDmVal[8]**

Offset 0x0690 - Enable SATA Port DmVal DITO multiplier.

Default is 15.

Definition at line 1611 of file FspsUpd.h.

**8.6.2.156   UINT8 FSP\_S\_CONFIG::SataPortsEnable[8]**

Offset 0x0042 - Enable SATA ports Enable/disable SATA ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line 206 of file FspsUpd.h.

**8.6.2.157   UINT8 FSP\_S\_CONFIG::SataPwrOptEnable**

Offset 0x065D - PCH Sata Pwr Opt Enable SATA Power Optimizer on PCH side.

\$EN\_DIS

Definition at line 1565 of file FspsUpd.h.

**8.6.2.158   UINT8 FSP\_S\_CONFIG::SataRstHddUnlock**

Offset 0x06B8 - PCH Sata Rst Hdd Unlock Indicates that the HDD password unlock in the OS is enabled.

\$EN\_DIS

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Definition at line 1674 of file FspsUpd.h.

#### 8.6.2.159 UINT8 FSP\_S\_CONFIG::SataRstIrrt

Offset 0x06B5 - PCH Sata Rst Irrt Intel Rapid Recovery Technology.

\$EN\_DIS

Definition at line 1657 of file FspsUpd.h.

#### 8.6.2.160 UINT8 FSP\_S\_CONFIG::SataRstIrrtOnly

Offset 0x06BA - PCH Sata Rst Irrt Only Allow only IRRT drives to span internal and external ports.

\$EN\_DIS

Definition at line 1687 of file FspsUpd.h.

#### 8.6.2.161 UINT8 FSP\_S\_CONFIG::SataRstLedLocate

Offset 0x06B9 - PCH Sata Rst Led Locate Indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

\$EN\_DIS

Definition at line 1681 of file FspsUpd.h.

#### 8.6.2.162 UINT8 FSP\_S\_CONFIG::SataRstOromUiBanner

Offset 0x06B6 - PCH Sata Rst Orom Ui Banner OROM UI and BANNER.

\$EN\_DIS

Definition at line 1663 of file FspsUpd.h.

#### 8.6.2.163 UINT8 FSP\_S\_CONFIG::SataRstPcieDeviceResetDelay[3]

Offset 0x06C2 - PCH Sata Rst Pcie Device Reset Delay PCIe Storage Device Reset Delay in milliseconds.

Default value is 100ms

Definition at line 1708 of file FspsUpd.h.

#### 8.6.2.164 UINT8 FSP\_S\_CONFIG::SataRstRaid0

Offset 0x06B1 - PCH Sata Rst Raid0 RAID0.

\$EN\_DIS

Definition at line 1633 of file FspsUpd.h.

#### 8.6.2.165 UINT8 FSP\_S\_CONFIG::SataRstRaid1

Offset 0x06B2 - PCH Sata Rst Raid1 RAID1.

\$EN\_DIS

Definition at line 1639 of file FspsUpd.h.

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**8.6.2.166   UINT8 FSP\_S\_CONFIG::SataRstRaid10**

Offset 0x06B3 - PCH Sata Rst Raid10 RAID10.

\$EN\_DIS

Definition at line 1645 of file FspUpd.h.

**8.6.2.167   UINT8 FSP\_S\_CONFIG::SataRstRaid5**

Offset 0x06B4 - PCH Sata Rst Raid5 RAID5.

\$EN\_DIS

Definition at line 1651 of file FspUpd.h.

**8.6.2.168   UINT8 FSP\_S\_CONFIG::SataRstRaidAlternateId**

Offset 0x06B0 - PCH Sata Rst Raid Alternate Id Enable RAID Alternate ID.

0:Client, 1:Alternate, 2:Server

Definition at line 1627 of file FspUpd.h.

**8.6.2.169   UINT8 FSP\_S\_CONFIG::SataRstSmartStorage**

Offset 0x06BB - PCH Sata Rst Smart Storage RST Smart Storage caching Bit.

\$EN\_DIS

Definition at line 1693 of file FspUpd.h.

**8.6.2.170   UINT8 FSP\_S\_CONFIG::SataSalpSupport**

Offset 0x0041 - Enable SATA SALP Support Enable/disable SATA Aggressive Link Power Management.

\$EN\_DIS

Definition at line 200 of file FspUpd.h.

**8.6.2.171   UINT8 FSP\_S\_CONFIG::SataThermalSuggestedSetting**

Offset 0x06FA - Sata Thermal Throttling Suggested Setting Sata Thermal Throttling Suggested Setting.

\$EN\_DIS

Definition at line 1942 of file FspUpd.h.

**8.6.2.172   UINT8 FSP\_S\_CONFIG::ScIrqSelect**

Offset 0x0088 - Select ScIrqSelect SCI IRQ Select.

The valid value is 9, 10, 11, and 20, 21, 22, 23 for APIC only.

Definition at line 275 of file FspUpd.h.

**8.6.2.173   UINT8 FSP\_S\_CONFIG::ScsEmmcEnabled**

Offset 0x0031 - Enable eMMC Controller Enable/disable eMMC Controller.

\$EN\_DIS

---

Definition at line 143 of file FspsUpd.h.

#### 8.6.2.174 UINT8 FSP\_S\_CONFIG::ScsEmmcHs400Enabled

Offset 0x0032 - Enable eMMC HS400 Mode Enable eMMC HS400 Mode.

\$EN\_DIS

Definition at line 149 of file FspsUpd.h.

#### 8.6.2.175 UINT8 FSP\_S\_CONFIG::ScsSdCardEnabled

Offset 0x0033 - Enable SdCard Controller Enable/disable SD Card Controller.

\$EN\_DIS

Definition at line 155 of file FspsUpd.h.

#### 8.6.2.176 UINT64 FSP\_S\_CONFIG::SendEcCmd

Offset 0x0730 - SendEcCmd SendEcCmd function pointer.

```
typedef EFI_STATUS (EFI_API *PLATFORM_SEND_EC_COMMAND) (IN EC_COMMAND_TYPE
EcCmdType, IN UINT8 EcCmd, IN UINT8 SendData, IN OUT UINT8 *ReceiveData);
```

Definition at line 2053 of file FspsUpd.h.

#### 8.6.2.177 UINT8 FSP\_S\_CONFIG::SendVrMbxCmd

Offset 0x02E2 - Enable VR specific mailbox command VR specific mailbox commands.

**00b - no VR specific command sent.** 01b - A VR mailbox command specifically for the MPS IMPV8 VR will be sent. 10b - VR specific command sent for PS4 exit issue. 11b - Reserved. \$EN\_DIS

Definition at line 762 of file FspsUpd.h.

#### 8.6.2.178 UINT8 FSP\_S\_CONFIG::SendVrMbxCmd1

Offset 0x02E3 - Select VR specific mailbox command to send VR specific mailbox commands.

**000b - no VR specific command sent.** 001b - VR mailbox command specifically for the MPS IMPV8 VR will be sent. 010b - VR specific command sent for PS4 exit issue. 100b - VR specific command sent for MPS VR decay issue.

Definition at line 769 of file FspsUpd.h.

#### 8.6.2.179 UINT8 FSP\_S\_CONFIG::SerialIoDebugUartNumber

Offset 0x06D6 - UART Number For Debug Purpose UART number for debug purpose.

0:UART0, 1: UART1, 2:UART2.

Definition at line 1762 of file FspsUpd.h.

**8.6.2.180** `UINT8 FSP_S_CONFIG::SerialIoDevMode[11]`

Offset 0x0074 - Enable SerialIo Device Mode 0:Disabled, 1:ACPI Mode, 2:PCI Mode, 3:Hidden mode, 4:Legacy UART mode - Enable/disable SerialIo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5,SPI0,SPI1,UART0,UART1,UART2 device mode respectively.

One byte for each controller, byte0 for I2C0, byte1 for I2C1, and so on.

Definition at line 258 of file FspUpd.h.

**8.6.2.181** `UINT8 FSP_S_CONFIG::SerialIoGpio`

Offset 0x06CA - Enable Pch Serial IO GPIO Determines if enable Serial IO GPIO.

\$EN\_DIS

Definition at line 1741 of file FspUpd.h.

**8.6.2.182** `UINT8 FSP_S_CONFIG::SerialIoI2cVoltage[6]`

Offset 0x06CB - IO voltage for I2C controllers Selects the IO voltage for I2C controllers, 0: PchSerialIoIs33V, 1: PchSerialIoIs18V.

Note: I2C 2/3/4/5 does not support 3.3V (only 1.8V), due to GPIO GPP\_F limitation

Definition at line 1747 of file FspUpd.h.

**8.6.2.183** `UINT8 FSP_S_CONFIG::ShowSpiController`

Offset 0x0035 - Show SPI controller Enable/disable to show SPI controller.

\$EN\_DIS

Definition at line 167 of file FspUpd.h.

**8.6.2.184** `UINT8 FSP_S_CONFIG::SlowSlewRateForGt`

Offset 0x027B - Slew Rate configuration for Deep Package C States for VR GT domain Slew Rate configuration for Deep Package C States for VR GT domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2**; 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line 664 of file FspUpd.h.

**8.6.2.185** `UINT8 FSP_S_CONFIG::SlowSlewRateForIa`

Offset 0x027A - Slew Rate configuration for Deep Package C States for VR IA domain Slew Rate configuration for Deep Package C States for VR IA domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2**; 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line 657 of file FspUpd.h.

**8.6.2.186** `UINT8 FSP_S_CONFIG::SlowSlewRateForSa`

Offset 0x027C - Slew Rate configuration for Deep Package C States for VR SA domain Slew Rate configuration for Deep Package C States for VR SA domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2**; 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line 671 of file FspUpd.h.

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**8.6.2.187    UINT8 FSP\_S\_CONFIG::SpiFlashCfgLockDown**

Offset 0x0036 - Flash Configuration Lock Down Enable/disable flash lock down.

If platform decides to skip this programming, it must lock SPI flash register DLOCK, FLOCKDN, and WRSDIS before end of post. \$EN\_DIS

Definition at line 174 of file FspsUpd.h.

**8.6.2.188    UINT8 FSP\_S\_CONFIG::SsicPortEnable**

Offset 0x006D - Enable XHCI SSIC Enable Enable/disable XHCI SSIC port.

\$EN\_DIS

Definition at line 236 of file FspsUpd.h.

**8.6.2.189    UINT8 FSP\_S\_CONFIG::TcolrqSelect**

Offset 0x0089 - Select TcolrqSelect TCO IRQ Select.

The valid value is 9, 10, 11, 20, 21, 22, 23.

Definition at line 280 of file FspsUpd.h.

**8.6.2.190    UINT16 FSP\_S\_CONFIG::TdcPowerLimit[5]**

Offset 0x0286 - Thermal Design Current current limit PCODE MMIO Mailbox: Thermal Design Current current limit.

Specified in 1/8A units. Range is 0-4095. 1000 = 125A. **0: Auto.** For all VR Indexes

Definition at line 681 of file FspsUpd.h.

**8.6.2.191    UINT8 FSP\_S\_CONFIG::TdcTimeWindow[5]**

Offset 0x026C - HECI3 state PCODE MMIO Mailbox: Thermal Design Current time window.

Defined in milli seconds. Valid Values 1 - 1ms , 2 - 2ms , 3 - 3ms , 4 - 4ms , 5 - 5ms , 6 - 6ms , 7 - 7ms , 8 - 8ms , 10 - 10ms. For all VR Indexe

Definition at line 619 of file FspsUpd.h.

**8.6.2.192    UINT8 FSP\_S\_CONFIG::TTSuggestedSetting**

Offset 0x06E6 - Thermal Throttling Suggested Setting Thermal Throttling Suggested Setting.

\$EN\_DIS

Definition at line 1836 of file FspsUpd.h.

**8.6.2.193    UINT8 FSP\_S\_CONFIG::TurboMode**

Offset 0x0040 - Turbo Mode Enable/Disable Turbo mode.

0: disable, 1: enable \$EN\_DIS

Definition at line 194 of file FspsUpd.h.

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**8.6.2.194** `UINT8 FSP_S_CONFIG::Usb2AfePehalfbit[16]`

Offset 0x00C3 - USB Per Port Half Bit Pre-emphasis USB Per Port Half Bit Pre-emphasis.

1b - half-bit pre-emphasis, 0b - full-bit pre-emphasis. One byte for each port.

Definition at line 336 of file FspsUpd.h.

**8.6.2.195** `UINT8 FSP_S_CONFIG::Usb2AfePetxiset[16]`

Offset 0x0093 - USB Per Port HS Preemphasis Bias USB Per Port HS Preemphasis Bias.

000b-0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV, 100b-28.15mV, 101b-39.35mV, 110b-45mV, 111b-56.↔  
3mV. One byte for each port.

Definition at line 318 of file FspsUpd.h.

**8.6.2.196** `UINT8 FSP_S_CONFIG::Usb2AfePredeemp[16]`

Offset 0x00B3 - USB Per Port HS Transmitter Emphasis USB Per Port HS Transmitter Emphasis.

00b - Emphasis OFF, 01b - De-emphasis ON, 10b - Pre-emphasis ON, 11b - Pre-emphasis & De-emphasis ON.  
One byte for each port.

Definition at line 330 of file FspsUpd.h.

**8.6.2.197** `UINT8 FSP_S_CONFIG::Usb2AfeTxiset[16]`

Offset 0x00A3 - USB Per Port HS Transmitter Bias USB Per Port HS Transmitter Bias.

000b-0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV, 100b-28.15mV, 101b-39.35mV, 110b-45mV, 111b-56.↔  
3mV, One byte for each port.

Definition at line 324 of file FspsUpd.h.

**8.6.2.198** `UINT8 FSP_S_CONFIG::Usb3HsioTxDeEmph[10]`

Offset 0x00DD - USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Setting USB 3.0 TX Output -3.5dB De-↔  
Emphasis Adjustment Setting, HSIO\_TX\_DWORD5[21:16], **Default = 29h** (approximately -3.5dB De-Emphasis).

One byte for each port.

Definition at line 348 of file FspsUpd.h.

**8.6.2.199** `UINT8 FSP_S_CONFIG::Usb3HsioTxDeEmphEnable[10]`

Offset 0x00D3 - Enable the write to USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Enable the write to USB  
3.0 TX Output -3.5dB De-Emphasis Adjustment.

Each value in array can be between 0-1. One byte for each port.

Definition at line 342 of file FspsUpd.h.

**8.6.2.200** `UINT8 FSP_S_CONFIG::Usb3HsioTxDownscaleAmp[10]`

Offset 0x00F1 - USB 3.0 TX Output Downscale Amplitude Adjustment USB 3.0 TX Output Downscale Amplitude  
Adjustment, HSIO\_TX\_DWORD8[21:16], **Default = 00h**.

One byte for each port.

Definition at line 360 of file FspsUpd.h.

**8.6.2.201    UINT8 FSP\_S\_CONFIG::Usb3HsioTxDownscaleAmpEnable[10]**

Offset 0x00E7 - Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment, Each value in array can be between 0-1.

One byte for each port.

Definition at line 354 of file FspsUpd.h.

**8.6.2.202    UINT32 FSP\_S\_CONFIG::VrPowerDeliveryDesign**

Offset 0x0290 - CPU VR Power Delivery Design Used to communicate the power delivery design capability of the board.

This value is an enum of the available power delivery segments that are defined in the Platform Design Guide.

Definition at line 688 of file FspsUpd.h.

**8.6.2.203    UINT16 FSP\_S\_CONFIG::VrVoltageLimit[5]**

Offset 0x02D4 - VR Voltage Limit PCODE MMIO Mailbox: VR Voltage Limit.

Range is 0-7999mV.

Definition at line 732 of file FspsUpd.h.

**8.6.2.204    UINT8 FSP\_S\_CONFIG::WatchDog**

Offset 0x0154 - WatchDog Timer Switch Enable/Disable.

0: Disable, 1: enable, Enable or disable WatchDog timer. \$EN\_DIS

Definition at line 416 of file FspsUpd.h.

**8.6.2.205    UINT16 FSP\_S\_CONFIG::WatchDogTimerBios**

Offset 0x015A - BIOS Timer 16 bits Value, Set BIOS watchdog timer.

\$EN\_DIS

Definition at line 447 of file FspsUpd.h.

**8.6.2.206    UINT16 FSP\_S\_CONFIG::WatchDogTimerOs**

Offset 0x0158 - OS Timer 16 bits Value, Set OS watchdog timer.

\$EN\_DIS

Definition at line 441 of file FspsUpd.h.

**8.6.2.207    UINT8 FSP\_S\_CONFIG::XdciEnable**

Offset 0x006C - Enable xDCI controller Enable/disable to xDCI controller.

\$EN\_DIS

Definition at line 230 of file FspsUpd.h.

The documentation for this struct was generated from the following file:

- [FspsUpd.h](#)

## 8.7 FSP\_S\_TEST\_CONFIG Struct Reference

Fsp S Test Configuration.

```
#include <FspSUpd.h>
```

### Public Attributes

- [UINT32 Signature](#)  
*Offset 0x0780.*
- [UINT8 ChapDeviceEnable](#)  
*Offset 0x0784 - Enable/Disable Device 7 Enable: Device 7 enabled, Disable (Default): Device 7 disabled \$EN\_DIS.*
- [UINT8 SkipPamLock](#)  
*Offset 0x0785 - Skip PAM register lock Enable: PAM register will not be locked by RC, platform code should lock it, Disable(Default): PAM registers will be locked by RC \$EN\_DIS.*
- [UINT8 EdramTestMode](#)  
*Offset 0x0786 - EDram Test Mode Enable: PAM register will not be locked by RC, platform code should lock it, Disable(Default): PAM registers will be locked by RC 0: EDram SW disable, 1: EDram SW Enable, 2: EDram HW mode.*
- [UINT8 DmiExtSync](#)  
*Offset 0x0787 - DMI Extended Sync Control Enable: Enable DMI Extended Sync Control, Disable(Default): Disable DMI Extended Sync Control \$EN\_DIS.*
- [UINT8 DmiIot](#)  
*Offset 0x0788 - DMI IOT Control Enable: Enable DMI IOT Control, Disable(Default): Disable DMI IOT Control \$EN←\_DIS.*
- [UINT8 PegMaxPayload \[3\]](#)  
*Offset 0x0789 - PEG Max Payload size per root port 0xFF(Default):Auto, 0x1: Force 128B, 0x2: Force 256B 0xFF: Auto, 0x1: Force 128B, 0x2: Force 256B.*
- [UINT8 RenderStandby](#)  
*Offset 0x078C - Enable/Disable IGFX RenderStandby Enable(Default): Enable IGFX RenderStandby, Disable: Disable IGFX RenderStandby \$EN\_DIS.*
- [UINT8 PmSupport](#)  
*Offset 0x078D - Enable/Disable IGFX PmSupport Enable(Default): Enable IGFX PmSupport, Disable: Disable IGFX PmSupport \$EN\_DIS.*
- [UINT8 CdynmaxClampEnable](#)  
*Offset 0x078E - Enable/Disable CdynmaxClamp Enable(Default): Enable CdynmaxClamp, Disable: Disable CdynmaxClamp \$EN\_DIS.*
- [UINT8 VtdDisable](#)  
*Offset 0x078F - Disable VT-d 0=Enable/FALSE(VT-d disabled), 1=Disable/TRUE (VT-d enabled) \$EN\_DIS.*
- [UINT8 GtFreqMax](#)  
*Offset 0x0790 - GT Frequency Limit 0xFF: Auto(Default), 2: 100 Mhz, 3: 150 Mhz, 4: 200 Mhz, 5: 250 Mhz, 6: 300 Mhz, 7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA: 500 Mhz, 0xB: 550 Mhz, 0xC: 600 Mhz, 0xD: 650 Mhz, 0xE: 700 Mhz, 0xF: 750 Mhz, 0x10: 800 Mhz, 0x11: 850 Mhz, 0x12:900 Mhz, 0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050 Mhz, 0x16: 1100 Mhz, 0x17: 1150 Mhz, 0x18: 1200 Mhz 0xFF: Auto(Default), 2: 100 Mhz, 3: 150 Mhz, 4: 200 Mhz, 5: 250 Mhz, 6: 300 Mhz, 7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA: 500 Mhz, 0xB: 550 Mhz, 0xC: 600 Mhz, 0xD: 650 Mhz, 0xE: 700 Mhz, 0xF: 750 Mhz, 0x10: 800 Mhz, 0x11: 850 Mhz, 0x12:900 Mhz, 0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050 Mhz, 0x16: 1100 Mhz, 0x17: 1150 Mhz, 0x18: 1200 Mhz.*
- [UINT8 SaPostMemTestRsvd \[11\]](#)  
*Offset 0x0791 - SaPostMemTestRsvd Reserved for SA Post-Mem Test \$EN\_DIS.*
- [UINT8 OneCoreRatioLimit](#)  
*Offset 0x079C - 1-Core Ratio Limit 1-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.*
- [UINT8 TwoCoreRatioLimit](#)  
*Offset 0x079D - 2-Core Ratio Limit 2-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.*
- [UINT8 ThreeCoreRatioLimit](#)

- Offset 0x079E - 3-Core Ratio Limit 3-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

    - UIN8 [FourCoreRatioLimit](#)
  - Offset 0x079F - 4-Core Ratio Limit 4-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

    - UIN8 [UnusedUpdSpace22](#)
  - Offset 0x07A0.

    - UIN8 [Hwp](#)
  - Offset 0x07A1 - Enable or Disable HWP Enable or Disable HWP(Hardware P states) Support.

    - UIN8 [HdcControl](#)
  - Offset 0x07A2 - Hardware Duty Cycle Control Hardware Duty Cycle Control configuration.

    - UIN8 [PowerLimit1Time](#)
  - Offset 0x07A3 - Package Long duration turbo mode time Package Long duration turbo mode time window in seconds.

    - UIN8 [PowerLimit2](#)
  - Offset 0x07A4 - Short Duration Turbo Mode Enable or Disable short duration Turbo Mode.

    - UIN8 [TurboPowerLimitLock](#)
  - Offset 0x07A5 - Turbo settings Lock Lock all Turbo settings Enable/Disable; **0: Disable** , **1: Enable** \$EN\_DIS.

    - UIN8 [PowerLimit3Time](#)
  - Offset 0x07A6 - Package PL3 time window Package PL3 time window range for this policy in milliseconds.

    - UIN8 [PowerLimit3DutyCycle](#)
  - Offset 0x07A7 - Package PL3 Duty Cycle Package PL3 Duty Cycle; Valid Range is 0 to 100.

    - UIN8 [PowerLimit3Lock](#)
  - Offset 0x07A8 - Package PL3 Lock Package PL3 Lock Enable/Disable; **0: Disable** ; **1: Enable** \$EN\_DIS.

    - UIN8 [PowerLimit4Lock](#)
  - Offset 0x07A9 - Package PL4 Lock Package PL4 Lock Enable/Disable; **0: Disable** ; **1: Enable** \$EN\_DIS.

    - UIN8 [TccActivationOffset](#)
  - Offset 0x07AA - TCC Activation Offset TCC Activation Offset.

    - UIN8 [TccOffsetClamp](#)
  - Offset 0x07AB - Tcc Offset Clamp Enable/Disable Tcc Offset Clamp for Runtime Average Temperature Limit (RATL) allows CPU to throttle below P1.For SKL Y SKU, the recommended default for this policy is **1: Enabled**, For all other SKUs the recommended default are **0: Disabled**.

    - UIN8 [TccOffsetLock](#)
  - Offset 0x07AC - Tcc Offset Lock Tcc Offset Lock for Runtime Average Temperature Limit (RATL) to lock temperature target; **0: Disabled**; **1: Enabled**.

    - UIN8 [NumberOfEntries](#)
  - Offset 0x07AD - Custom Ratio State Entries The number of custom ratio state entries, ranges from 0 to 40 for a valid custom ratio table.Sets the number of custom P-states.

    - UIN8 [Custom1PowerLimit1Time](#)
  - Offset 0x07AE - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTD level 1.

    - UIN8 [Custom1TurboActivationRatio](#)
  - Offset 0x07AF - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 1.

    - UIN8 [Custom1ConfigTdpControl](#)
  - Offset 0x07B0 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

    - UIN8 [Custom2PowerLimit1Time](#)
  - Offset 0x07B1 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTD level 2.

    - UIN8 [Custom2TurboActivationRatio](#)
  - Offset 0x07B2 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 2.

    - UIN8 [Custom2ConfigTdpControl](#)
  - Offset 0x07B3 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

    - UIN8 [Custom3PowerLimit1Time](#)
  - Offset 0x07B4 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTD level 3.
-



- UINT8 [Custom3TurboActivationRatio](#)  
Offset 0x07B5 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 3.
  - UINT8 [Custom3ConfigTdpControl](#)  
Offset 0x07B6 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.
  - UINT8 [ConfigTdpLock](#)  
Offset 0x07B7 - ConfigTdp mode settings Lock Lock the ConfigTdp mode settings from runtime changes; **0: Disable**; 1: Enable \$EN\_DIS.
  - UINT8 [ConfigTdpBios](#)  
Offset 0x07B8 - Load Configurable TDP SSDT Configure whether to load Configurable TDP SSDT; **0: Disable**; 1: Enable.
  - UINT8 [PsysPowerLimit1](#)  
Offset 0x07B9 - PL1 Enable value PL1 Enable value to limit average platform power.
  - UINT8 [PsysPowerLimit1Time](#)  
Offset 0x07BA - PL1 timewindow PL1 timewindow in seconds. Valid values (Unit in seconds) 0 to 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128.
  - UINT8 [PsysPowerLimit2](#)  
Offset 0x07BB - PL2 Enable Value PL2 Enable activates the PL2 value to limit average platform power.
  - UINT8 [UnusedUpdSpace23](#) [2]  
Offset 0x07BC.
  - UINT8 [MlcStreamerPrefetcher](#)  
Offset 0x07BE - Enable or Disable MLC Streamer Prefetcher Enable or Disable MLC Streamer Prefetcher; 0: Disable; **1: Enable**.
  - UINT8 [MlcSpatialPrefetcher](#)  
Offset 0x07BF - Enable or Disable MLC Spatial Prefetcher Enable or Disable MLC Spatial Prefetcher; 0: Disable; **1: Enable** \$EN\_DIS.
  - UINT8 [MonitorMwaitEnable](#)  
Offset 0x07C0 - Enable or Disable Monitor /MWAIT instructions Enable or Disable Monitor /MWAIT instructions; 0: Disable; **1: Enable**.
  - UINT8 [MachineCheckEnable](#)  
Offset 0x07C1 - Enable or Disable initialization of machine check registers Enable or Disable initialization of machine check registers; 0: Disable; **1: Enable**.
  - UINT8 [DebugInterfaceEnable](#)  
Offset 0x07C2 - Enable or Disable processor debug features Enable or Disable processor debug features; **0: Disable**; 1: Enable.
  - UINT8 [DebugInterfaceLockEnable](#)  
Offset 0x07C3 - Lock or Unlock debug interface features Lock or Unlock debug interface features; 0: Disable; **1: Enable**.
  - UINT8 [AplIdleManner](#)  
Offset 0x07C4 - AP Idle Manner of waiting for SIPI AP Idle Manner of waiting for SIPI; 1: HALT loop; **2: MWAIT loop**; 3: RUN loop.
  - UINT8 [ApHandoffManner](#)  
Offset 0x07C5 - Settings for AP Handoff to OS Settings for AP Handoff to OS; 1: HALT loop; **2: MWAIT loop**.
  - UINT8 [UnusedUpdSpace24](#) [2]  
Offset 0x07C6.
  - UINT8 [ProcTraceOutputScheme](#)  
Offset 0x07C8 - Control on Processor Trace output scheme Control on Processor Trace output scheme; **0: Single Range Output**; 1: ToPA Output.
  - UINT8 [ProcTraceEnable](#)  
Offset 0x07C9 - Enable or Disable Processor Trace feature Enable or Disable Processor Trace feature; **0: Disable**; 1: Enable.
  - UINT8 [ProcTraceMemSize](#)
-

Offset 0x07CA - Memory region allocation for Processor Trace Memory region allocation for Processor Trace, Total Memory required is up to requested value \* 2 (for memory alignment) \* 8 active threads, to enable Processor Trace, PcdFspReservedMemoryLength must be increased by the total memory required, and PlatformMemorySize policy must also be increased by the total memory required over 32MB, Valid Values are 0 - 4KB , 0x1 - 8KB , 0x2 - 16KB , 0x3 - 32KB , 0x4 - 64KB , 0x5 - 128KB , 0x6 - 256KB , 0x7 - 512KB , 0x8 - 1MB , 0x9 - 2MB , 0xA - 4MB , 0xB - 8MB , 0xC - 16MB , 0xD - 32MB , 0xE - 64MB , 0xF - 128MB , 0xFF: Disable.

- UINT8 [UnusedUpdSpace25](#)

Offset 0x07CB.

- UINT8 [VoltageOptimization](#)

Offset 0x07CC - Enable or Disable Voltage Optimization feature Enable or Disable Voltage Optimization feature 0: Disable; **1: Enable** \$EN\_DIS.

- UINT8 [Eist](#)

Offset 0x07CD - Enable or Disable Intel SpeedStep Technology Enable or Disable Intel SpeedStep Technology.

- UINT8 [EnergyEfficientPState](#)

Offset 0x07CE - Enable or Disable Energy Efficient P-state Enable or Disable Energy Efficient P-state will be applied in Turbo mode.

- UINT8 [EnergyEfficientTurbo](#)

Offset 0x07CF - Enable or Disable Energy Efficient Turbo Enable or Disable Energy Efficient Turbo, will be applied in Turbo mode.

- UINT8 [TStates](#)

Offset 0x07D0 - Enable or Disable T states Enable or Disable T states; **0: Disable**; 1: Enable.

- UINT8 [BiProcHot](#)

Offset 0x07D1 - Enable or Disable Bi-Directional PROCHOT# Enable or Disable Bi-Directional PROCHOT#; 0: Disable; **1: Enable** \$EN\_DIS.

- UINT8 [DisableProcHotOut](#)

Offset 0x07D2 - Enable or Disable PROCHOT# signal being driven externally Enable or Disable PROCHOT# signal being driven externally; 0: Disable; **1: Enable**.

- UINT8 [ProcHotResponse](#)

Offset 0x07D3 - Enable or Disable PROCHOT# Response Enable or Disable PROCHOT# Response; **0: Disable**; 1: Enable.

- UINT8 [DisableVrThermalAlert](#)

Offset 0x07D4 - Enable or Disable VR Thermal Alert Enable or Disable VR Thermal Alert; **0: Disable**; 1: Enable.

- UINT8 [AutoThermalReporting](#)

Offset 0x07D5 - Enable or Disable Thermal Reporting Enable or Disable Thermal Reporting through ACPI tables; 0: Disable; **1: Enable**.

- UINT8 [ThermalMonitor](#)

Offset 0x07D6 - Enable or Disable Thermal Monitor Enable or Disable Thermal Monitor; 0: Disable; **1: Enable** \$EN\_DIS.

- UINT8 [Cx](#)

Offset 0x07D7 - Enable or Disable CPU power states (C-states) Enable or Disable CPU power states (C-states).

- UINT8 [PmgCstCfgCtrlLock](#)

Offset 0x07D8 - Configure C-State Configuration Lock Configure C-State Configuration Lock; 0: Disable; **1: Enable**.

- UINT8 [C1e](#)

Offset 0x07D9 - Enable or Disable Enhanced C-states Enable or Disable Enhanced C-states.

- UINT8 [PkgCStateDemotion](#)

Offset 0x07DA - Enable or Disable Package C-State Demotion Enable or Disable Package C-State Demotion.

- UINT8 [PkgCStateUnDemotion](#)

Offset 0x07DB - Enable or Disable Package C-State UnDemotion Enable or Disable Package C-State UnDemotion.

- UINT8 [CStatePreWake](#)

Offset 0x07DC - Enable or Disable CState-Pre wake Enable or Disable CState-Pre wake.

- UINT8 [TimedMwait](#)

Offset 0x07DD - Enable or Disable TimedMwait Support.

- UINT8 [CstCfgCtrlMwaitRedirection](#)

Offset 0x07DE - Enable or Disable IO to MWAIT redirection Enable or Disable IO to MWAIT redirection; **0: Disable**; 1: Enable.

- UINT8 [PkgCStateLimit](#)

Offset 0x07DF - Set the Max Pkg Cstate Set the Max Pkg Cstate.

- UINT8 [CstateLatencyControl0TimeUnit](#)

Offset 0x07E0 - TimeUnit for C-State Latency Control0 TimeUnit for C-State Latency Control0; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [CstateLatencyControl1TimeUnit](#)

Offset 0x07E1 - TimeUnit for C-State Latency Control1 TimeUnit for C-State Latency Control1; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [CstateLatencyControl2TimeUnit](#)

Offset 0x07E2 - TimeUnit for C-State Latency Control2 TimeUnit for C-State Latency Control2; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [CstateLatencyControl3TimeUnit](#)

Offset 0x07E3 - TimeUnit for C-State Latency Control3 TimeUnit for C-State Latency Control3; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [CstateLatencyControl4TimeUnit](#)

Offset 0x07E4 - TimeUnit for C-State Latency Control4 TimeUnit for C-State Latency Control4; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [CstateLatencyControl5TimeUnit](#)

Offset 0x07E5 - TimeUnit for C-State Latency Control5 TimeUnit for C-State Latency Control5; Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 - 33554432ns.

- UINT8 [PpmIrmSetting](#)

Offset 0x07E6 - Interrupt Redirection Mode Select Interrupt Redirection Mode Select.0: Fixed priority; 1: Round robin; 2: Hash vector; 4: PAIR with fixed priority; 5: PAIR with round robin; 6: PAIR with hash vector; 7: No change.

- UINT8 [ProcHotLock](#)

Offset 0x07E7 - Lock prohot configuration Lock prohot configuration Enable/Disable; **0: Disable**; 1: Enable \$EN↔\_DIS.

- UINT8 [ConfigTdpLevel](#)

Offset 0x07E8 - Configuration for boot TDP selection Configuration for boot TDP selection; **0: TDP Nominal**; 1: TDP Down; 2: TDP Up; 0xFF: Deactivate 0:TDP Nominal, 1:TDP Down, 2:TDP Up, 0xFF:Deactivate.

- UINT8 [RaceToHalt](#)

Offset 0x07E9 - Race To Halt Enable/Disable Race To Halt feature.

- UINT16 [MaxRatio](#)

Offset 0x07EA - Max P-State Ratio Max P-State Ratio , Valid Range 0 to 0x7F.

- UINT16 [StateRatio](#) [40]

Offset 0x07EC - Maximum P-state ratio to use in the custom P-state table Maximum P-state ratio to use in the custom P-state table.

- UINT16 [CstateLatencyControl0Irtl](#)

Offset 0x083C - Interrupt Response Time Limit of C-State LatencyControl0 Interrupt Response Time Limit of C-State LatencyControl0. Range of value 0 to 0x3FF, Default is 0x4E, Server Platform is 0x4B.

- UINT16 [CstateLatencyControl1Irtl](#)

Offset 0x083E - Interrupt Response Time Limit of C-State LatencyControl1 Interrupt Response Time Limit of C-State LatencyControl1. Range of value 0 to 0x3FF, Default is 0x76, Server Platform is 0x6B.

- UINT16 [CstateLatencyControl2Irtl](#)

Offset 0x0840 - Interrupt Response Time Limit of C-State LatencyControl2 Interrupt Response Time Limit of C-State LatencyControl2. Range of value 0 to 0x3FF.

- UINT16 [CstateLatencyControl3Irtl](#)

Offset 0x0842 - Interrupt Response Time Limit of C-State LatencyControl3 Interrupt Response Time Limit of C-State LatencyControl3. Range of value 0 to 0x3FF.

- UINT16 [CstateLatencyControl4Irtl](#)

Offset 0x0844 - Interrupt Response Time Limit of C-State LatencyControl4 Interrupt Response Time Limit of C-State LatencyControl4. Range of value 0 to 0x3FF.

- UINT16 [CstateLatencyControl5Irtl](#)

Offset 0x0846 - Interrupt Response Time Limit of C-State LatencyControl5 Interrupt Response Time Limit of C-State LatencyControl5. Range of value 0 to 0x3FF.

- UINT32 [PowerLimit1](#)  
Offset 0x0848 - Package Long duration turbo mode power limit Package Long duration turbo mode power limit.
- UINT32 [PowerLimit2Power](#)  
Offset 0x084C - Package Short duration turbo mode power limit Package Short duration turbo mode power limit.
- UINT32 [PowerLimit3](#)  
Offset 0x0850 - Package PL3 power limit Package PL3 power limit.
- UINT32 [PowerLimit4](#)  
Offset 0x0854 - Package PL4 power limit Package PL4 power limit.
- UINT32 [TccOffsetTimeWindowForRatl](#)  
Offset 0x0858 - Tcc Offset Time Window for RATL Package PL4 power limit.
- UINT32 [Custom1PowerLimit1](#)  
Offset 0x085C - Short term Power Limit value for custom cTDP level 1 Short term Power Limit value for custom cTDP level 1.
- UINT32 [Custom1PowerLimit2](#)  
Offset 0x0860 - Long term Power Limit value for custom cTDP level 1 Long term Power Limit value for custom cTDP level 1.
- UINT32 [Custom2PowerLimit1](#)  
Offset 0x0864 - Short term Power Limit value for custom cTDP level 2 Short term Power Limit value for custom cTDP level 2.
- UINT32 [Custom2PowerLimit2](#)  
Offset 0x0868 - Long term Power Limit value for custom cTDP level 2 Long term Power Limit value for custom cTDP level 2.
- UINT32 [Custom3PowerLimit1](#)  
Offset 0x086C - Short term Power Limit value for custom cTDP level 3 Short term Power Limit value for custom cTDP level 3.
- UINT32 [Custom3PowerLimit2](#)  
Offset 0x0870 - Long term Power Limit value for custom cTDP level 3 Long term Power Limit value for custom cTDP level 3.
- UINT32 [PsysPowerLimit1Power](#)  
Offset 0x0874 - Platform PL1 power Platform PL1 power.
- UINT32 [PsysPowerLimit2Power](#)  
Offset 0x0878 - Platform PL2 power Platform PL2 power.
- UINT16 [PsysPmax](#)  
Offset 0x087C - Platform Power Pmax PCODE MMIO Mailbox: Platform Power Pmax.
- UINT16 [CpuS3ResumeDataSize](#)  
Offset 0x087E - CpuS3ResumeDataSize Size of CPU S3 Resume Data.
- UINT32 [CpuS3ResumeData](#)  
Offset 0x0880 - CpuS3ResumeData Pointer to CPU S3 Resume Data.
- UINT8 [FiveCoreRatioLimit](#)  
Offset 0x0884 - 5-Core Ratio Limit 5-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.
- UINT8 [SixCoreRatioLimit](#)  
Offset 0x0885 - 6-Core Ratio Limit 6-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.
- UINT8 [SevenCoreRatioLimit](#)  
Offset 0x0886 - 7-Core Ratio Limit 7-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.
- UINT8 [EightCoreRatioLimit](#)  
Offset 0x0887 - 8-Core Ratio Limit 8-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.
- UINT8 [ThreeStrikeCounterDisable](#)  
Offset 0x0888 - Set Three Strike Counter Disable False (default): Three Strike counter will be incremented and True: Prevents Three Strike counter from incrementing; **0: False**; 1: True.
- UINT8 [ReservedCpuPostMemTest](#) [1]

- Offset 0x0889 - ReservedCpuPostMemTest Reserved for CPU Post-Mem Test \$EN\_DIS.
  - UINT8 [SgxSinitDataFromTpm](#)  
Offset 0x088A - SgxSinitDataFromTpm SgxSinitDataFromTpm default values.
  - UINT8 [EndOfPostMessage](#)  
Offset 0x088B - End of Post message Test, Send End of Post message.
  - UINT8 [DisableD0I3SettingForHeci](#)  
Offset 0x088C - D0I3 Setting for HECI Disable Test, 0: disable, 1: enable, Setting this option disables setting D0I3 bit for all HECI devices \$EN\_DIS.
  - UINT8 [PchLockDownGlobalSmi](#)  
Offset 0x088D - Enable LOCKDOWN SMI Enable SMI\_LOCK bit to prevent writes to the Global SMI Enable bit.
  - UINT16 [PchHdaResetWaitTimer](#)  
Offset 0x088E - HD Audio Reset Wait Timer The delay timer after Azalia reset, the value is number of microseconds.
  - UINT8 [PchLockDownBiosInterface](#)  
Offset 0x0890 - Enable LOCKDOWN BIOS Interface Enable BIOS Interface Lock Down bit to prevent writes to the Backup Control Register.
  - UINT8 [PchLockDownRtcLock](#)  
Offset 0x0891 - RTC CMOS RAM LOCK Enable RTC lower and upper 128 byte Lock bits to lock Bytes 38h-3Fh in the upper and and lower 128-byte bank of RTC RAM.
  - UINT8 [PchSbiUnlock](#)  
Offset 0x0892 - PCH Sbi lock bit This unlock the SBI lock bit to allow SBI after post time.
  - UINT8 [PchSbAccessUnlock](#)  
Offset 0x0893 - PCH Psf lock bit The PSF registers will be locked before 3rd party code execution.
  - UINT16 [PcieRpLtrMaxSnoopLatency](#) [24]  
Offset 0x0894 - PCIE RP Ltr Max Snoop Latency Latency Tolerance Reporting, Max Snoop Latency.
  - UINT16 [PcieRpLtrMaxNoSnoopLatency](#) [24]  
Offset 0x08C4 - PCIE RP Ltr Max No Snoop Latency Latency Tolerance Reporting, Max Non-Snoop Latency.
  - UINT8 [PcieRpSnoopLatencyOverrideMode](#) [24]  
Offset 0x08F4 - PCIE RP Snoop Latency Override Mode Latency Tolerance Reporting, Snoop Latency Override Mode.
  - UINT8 [PcieRpSnoopLatencyOverrideMultiplier](#) [24]  
Offset 0x090C - PCIE RP Snoop Latency Override Multiplier Latency Tolerance Reporting, Snoop Latency Override Multiplier.
  - UINT16 [PcieRpSnoopLatencyOverrideValue](#) [24]  
Offset 0x0924 - PCIE RP Snoop Latency Override Value Latency Tolerance Reporting, Snoop Latency Override Value.
  - UINT8 [PcieRpNonSnoopLatencyOverrideMode](#) [24]  
Offset 0x0954 - PCIE RP Non Snoop Latency Override Mode Latency Tolerance Reporting, Non-Snoop Latency Override Mode.
  - UINT8 [PcieRpNonSnoopLatencyOverrideMultiplier](#) [24]  
Offset 0x096C - PCIE RP Non Snoop Latency Override Multiplier Latency Tolerance Reporting, Non-Snoop Latency Override Multiplier.
  - UINT16 [PcieRpNonSnoopLatencyOverrideValue](#) [24]  
Offset 0x0984 - PCIE RP Non Snoop Latency Override Value Latency Tolerance Reporting, Non-Snoop Latency Override Value.
  - UINT8 [PcieRpSlotPowerLimitScale](#) [24]  
Offset 0x09B4 - PCIE RP Slot Power Limit Scale Specifies scale used for slot power limit value.
  - UINT16 [PcieRpSlotPowerLimitValue](#) [24]  
Offset 0x09CC - PCIE RP Slot Power Limit Value Specifies upper limit on power supply by slot.
  - UINT8 [PcieRpUptp](#) [24]  
Offset 0x09FC - PCIE RP Upstream Port Transmitter Preset Used during Gen3 Link Equalization.
  - UINT8 [PcieRpDptp](#) [24]  
Offset 0x0A14 - PCIE RP Downstream Port Transmitter Preset Used during Gen3 Link Equalization.
  - UINT8 [PcieEnablePort8xhDecode](#)
-

Offset 0x0A2C - PCIE RP Enable Port8xh Decode This member describes whether PCIE root port Port 8xh Decode is enabled.

- UINT8 [PchPciePort8xhDecodePortIndex](#)

Offset 0x0A2D - PCIE Port8xh Decode Port Index The Index of PCIe Port that is selected for Port8xh Decode (0 Based).

- UINT8 [PchPmDisableEnergyReport](#)

Offset 0x0A2E - PCH Pm Disable Energy Report Disable/Enable PCH to CPU enery report feature.

- UINT8 [PchPmPmcReadDisable](#)

Offset 0x0A2F - PCH Pm Pmc Read Disable Deprecated \$EN\_DIS.

- UINT8 [SataTestMode](#)

Offset 0x0A30 - PCH Sata Test Mode Allow entrance to the PCH SATA test modes.

- UINT8 [ReservedFspstestUpd](#) [15]

Offset 0x0A31.

### 8.7.1 Detailed Description

Fsp S Test Configuration.

Definition at line 2114 of file Fspstest.h.

### 8.7.2 Member Data Documentation

#### 8.7.2.1 UINT8 FSP\_S\_TEST\_CONFIG::ApHandoffManner

Offset 0x07C5 - Settings for AP Handoff to OS Settings for AP Handoff to OS; 1: HALT loop; **2: MWAIT loop.**

1:HALT loop, 2:MWAIT loop

Definition at line 2442 of file Fspstest.h.

#### 8.7.2.2 UINT8 FSP\_S\_TEST\_CONFIG::ApIdleManner

Offset 0x07C4 - AP Idle Manner of waiting for SIPI AP Idle Manner of waiting for SIPI; 1: HALT loop; **2: MWAIT loop**; 3: RUN loop.

1:HALT loop, 2:MWAIT loop, 3:RUN loop

Definition at line 2436 of file Fspstest.h.

#### 8.7.2.3 UINT8 FSP\_S\_TEST\_CONFIG::AutoThermalReporting

Offset 0x07D5 - Enable or Disable Thermal Reporting Enable or Disable Thermal Reporting through ACPI tables; 0: Disable; **1: Enable.**

\$EN\_DIS

Definition at line 2535 of file Fspstest.h.

#### 8.7.2.4 UINT8 FSP\_S\_TEST\_CONFIG::C1e

Offset 0x07D9 - Enable or Disable Enhanced C-states Enable or Disable Enhanced C-states.

0: Disable; **1: Enable** \$EN\_DIS

Definition at line 2559 of file Fspstest.h.

#### 8.7.2.5 UINT8 FSP\_S\_TEST\_CONFIG::ConfigTdpBios

Offset 0x07B8 - Load Configurable TDP SSDT Configure whether to load Configurable TDP SSDT; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2371 of file FspUpd.h.

#### 8.7.2.6 UINT8 FSP\_S\_TEST\_CONFIG::CStatePreWake

Offset 0x07DC - Enable or Disable CState-Pre wake Enable or Disable CState-Pre wake.

0: Disable; 1: **Enable** \$EN\_DIS

Definition at line 2579 of file FspUpd.h.

#### 8.7.2.7 UINT8 FSP\_S\_TEST\_CONFIG::CstCfgCtrlIoMwaitRedirection

Offset 0x07DE - Enable or Disable IO to MWAIT redirection Enable or Disable IO to MWAIT redirection; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2591 of file FspUpd.h.

#### 8.7.2.8 UINT8 FSP\_S\_TEST\_CONFIG::Custom1ConfigTdpControl

Offset 0x07B0 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line 2329 of file FspUpd.h.

#### 8.7.2.9 UINT32 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit1

Offset 0x085C - Short term Power Limit value for custom cTDP level 1 Short term Power Limit value for custom cTDP level 1.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2741 of file FspUpd.h.

#### 8.7.2.10 UINT8 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit1Time

Offset 0x07AE - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 1.

Valid Range 0 to 128

Definition at line 2319 of file FspUpd.h.

#### 8.7.2.11 UINT32 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit2

Offset 0x0860 - Long term Power Limit value for custom cTDP level 1 Long term Power Limit value for custom cTDP level 1.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2747 of file FspUpd.h.

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**8.7.2.12 UINT8 FSP\_S\_TEST\_CONFIG::Custom1TurboActivationRatio**

Offset 0x07AF - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 1.

Valid Range 0 to 255

Definition at line 2324 of file FspsUpd.h.

**8.7.2.13 UINT8 FSP\_S\_TEST\_CONFIG::Custom2ConfigTdpControl**

Offset 0x07B3 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line 2344 of file FspsUpd.h.

**8.7.2.14 UINT32 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit1**

Offset 0x0864 - Short term Power Limit value for custom cTDP level 2 Short term Power Limit value for custom cTDP level 2.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2753 of file FspsUpd.h.

**8.7.2.15 UINT8 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit1Time**

Offset 0x07B1 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 2.

Valid Range 0 to 128

Definition at line 2334 of file FspsUpd.h.

**8.7.2.16 UINT32 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit2**

Offset 0x0868 - Long term Power Limit value for custom cTDP level 2 Long term Power Limit value for custom cTDP level 2.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2759 of file FspsUpd.h.

**8.7.2.17 UINT8 FSP\_S\_TEST\_CONFIG::Custom2TurboActivationRatio**

Offset 0x07B2 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 2.

Valid Range 0 to 255

Definition at line 2339 of file FspsUpd.h.

**8.7.2.18 UINT8 FSP\_S\_TEST\_CONFIG::Custom3ConfigTdpControl**

Offset 0x07B6 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line 2359 of file FspsUpd.h.

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**8.7.2.19 UINT32 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit1**

Offset 0x086C - Short term Power Limit value for custom cTDP level 3 Short term Power Limit value for custom cTDP level 3.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2765 of file FspsUpd.h.

**8.7.2.20 UINT8 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit1Time**

Offset 0x07B4 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 3.

Valid Range 0 to 128

Definition at line 2349 of file FspsUpd.h.

**8.7.2.21 UINT32 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit2**

Offset 0x0870 - Long term Power Limit value for custom cTDP level 3 Long term Power Limit value for custom cTDP level 3.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2771 of file FspsUpd.h.

**8.7.2.22 UINT8 FSP\_S\_TEST\_CONFIG::Custom3TurboActivationRatio**

Offset 0x07B5 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 3.

Valid Range 0 to 255

Definition at line 2354 of file FspsUpd.h.

**8.7.2.23 UINT8 FSP\_S\_TEST\_CONFIG::Cx**

Offset 0x07D7 - Enable or Disable CPU power states (C-states) Enable or Disable CPU power states (C-states).

0: Disable; **1: Enable** \$EN\_DIS

Definition at line 2547 of file FspsUpd.h.

**8.7.2.24 UINT8 FSP\_S\_TEST\_CONFIG::DebugInterfaceEnable**

Offset 0x07C2 - Enable or Disable processor debug features Enable or Disable processor debug features; **0**↵: **Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2424 of file FspsUpd.h.

**8.7.2.25 UINT8 FSP\_S\_TEST\_CONFIG::DebugInterfaceLockEnable**

Offset 0x07C3 - Lock or Unlock debug interface features Lock or Unlock debug interface features; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line 2430 of file FspsUpd.h.

**8.7.2.26 UINT8 FSP\_S\_TEST\_CONFIG::DisableProcHotOut**

Offset 0x07D2 - Enable or Disable PROCHOT# signal being driven externally Enable or Disable PROCHOT# signal being driven externally; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line 2517 of file FspUpd.h.

**8.7.2.27 UINT8 FSP\_S\_TEST\_CONFIG::DisableVrThermalAlert**

Offset 0x07D4 - Enable or Disable VR Thermal Alert Enable or Disable VR Thermal Alert; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2529 of file FspUpd.h.

**8.7.2.28 UINT8 FSP\_S\_TEST\_CONFIG::EightCoreRatioLimit**

Offset 0x0887 - 8-Core Ratio Limit 8-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 8-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2823 of file FspUpd.h.

**8.7.2.29 UINT8 FSP\_S\_TEST\_CONFIG::Eist**

Offset 0x07CD - Enable or Disable Intel SpeedStep Technology Enable or Disable Intel SpeedStep Technology.

0: Disable; **1: Enable** \$EN\_DIS

Definition at line 2485 of file FspUpd.h.

**8.7.2.30 UINT8 FSP\_S\_TEST\_CONFIG::EndOfPostMessage**

Offset 0x088B - End of Post message Test, Send End of Post message.

Disable(0x0): Disable EOP message, Send in PEI(0x1): EOP send in PEI, Send in DXE(0x2)(Default): EOP send in PEI 0:Disable, 1:Send in PEI, 2:Send in DXE, 3:Reserved

Definition at line 2848 of file FspUpd.h.

**8.7.2.31 UINT8 FSP\_S\_TEST\_CONFIG::EnergyEfficientPState**

Offset 0x07CE - Enable or Disable Energy Efficient P-state Enable or Disable Energy Efficient P-state will be applied in Turbo mode.

Disable; **1: Enable** \$EN\_DIS

Definition at line 2492 of file FspUpd.h.

**8.7.2.32 UINT8 FSP\_S\_TEST\_CONFIG::EnergyEfficientTurbo**

Offset 0x07CF - Enable or Disable Energy Efficient Turbo Enable or Disable Energy Efficient Turbo, will be applied in Turbo mode.

Disable; **1: Enable** \$EN\_DIS

Definition at line 2499 of file FspUpd.h.

**8.7.2.33**  UINT8 FSP\_S\_TEST\_CONFIG::FiveCoreRatioLimit

Offset 0x0884 - 5-Core Ratio Limit 5-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 5-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2805 of file FspUpd.h.

**8.7.2.34**  UINT8 FSP\_S\_TEST\_CONFIG::FourCoreRatioLimit

Offset 0x079F - 4-Core Ratio Limit 4-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 4-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2227 of file FspUpd.h.

**8.7.2.35**  UINT8 FSP\_S\_TEST\_CONFIG::HdcControl

Offset 0x07A2 - Hardware Duty Cycle Control Hardware Duty Cycle Control configuration.

0: Disabled; **1: Enabled** 2-3:Reserved \$EN\_DIS

Definition at line 2244 of file FspUpd.h.

**8.7.2.36**  UINT8 FSP\_S\_TEST\_CONFIG::Hwp

Offset 0x07A1 - Enable or Disable HWP Enable or Disable HWP(Hardware P states) Support.

0: Disable; **1: Enable**; 2-3:Reserved \$EN\_DIS

Definition at line 2238 of file FspUpd.h.

**8.7.2.37**  UINT8 FSP\_S\_TEST\_CONFIG::MachineCheckEnable

Offset 0x07C1 - Enable or Disable initialization of machine check registers Enable or Disable initialization of machine check registers; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line 2418 of file FspUpd.h.

**8.7.2.38**  UINT8 FSP\_S\_TEST\_CONFIG::MlcStreamerPrefetcher

Offset 0x07BE - Enable or Disable MLC Streamer Prefetcher Enable or Disable MLC Streamer Prefetcher; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line 2400 of file FspUpd.h.

**8.7.2.39**  UINT8 FSP\_S\_TEST\_CONFIG::MonitorMwaitEnable

Offset 0x07C0 - Enable or Disable Monitor /MWAIT instructions Enable or Disable Monitor /MWAIT instructions; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line 2412 of file FspUpd.h.

#### 8.7.2.40 UINT8 FSP\_S\_TEST\_CONFIG::NumberOfEntries

Offset 0x07AD - Custom Ratio State Entries The number of custom ratio state entries, ranges from 0 to 40 for a valid custom ratio table. Sets the number of custom P-states.

At least 2 states must be present

Definition at line 2314 of file FspUpd.h.

#### 8.7.2.41 UINT8 FSP\_S\_TEST\_CONFIG::OneCoreRatioLimit

Offset 0x079C - 1-Core Ratio Limit 1-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 1-Core Ratio Limit Must be greater than or equal to 2-Core Ratio Limit, 3-Core Ratio Limit, 4-Core Ratio Limit, 5-Core Ratio Limit, 6-Core Ratio Limit, 7-Core Ratio Limit, 8-Core Ratio Limit. Range is 0 to 255

Definition at line 2209 of file FspUpd.h.

#### 8.7.2.42 UINT16 FSP\_S\_TEST\_CONFIG::PchHdaResetWaitTimer

Offset 0x088E - HD Audio Reset Wait Timer The delay timer after Azalia reset, the value is number of microseconds.

Default is 600.

Definition at line 2866 of file FspUpd.h.

#### 8.7.2.43 UINT8 FSP\_S\_TEST\_CONFIG::PchLockDownBiosInterface

Offset 0x0890 - Enable LOCKDOWN BIOS Interface Enable BIOS Interface Lock Down bit to prevent writes to the Backup Control Register.

\$EN\_DIS

Definition at line 2872 of file FspUpd.h.

#### 8.7.2.44 UINT8 FSP\_S\_TEST\_CONFIG::PchLockDownGlobalSmi

Offset 0x088D - Enable LOCKDOWN SMI Enable SMI\_LOCK bit to prevent writes to the Global SMI Enable bit.

\$EN\_DIS

Definition at line 2861 of file FspUpd.h.

#### 8.7.2.45 UINT8 FSP\_S\_TEST\_CONFIG::PchLockDownRtcLock

Offset 0x0891 - RTC CMOS RAM LOCK Enable RTC lower and upper 128 byte Lock bits to lock Bytes 38h-3Fh in the upper and lower 128-byte bank of RTC RAM.

\$EN\_DIS

Definition at line 2879 of file FspUpd.h.

#### 8.7.2.46 UINT8 FSP\_S\_TEST\_CONFIG::PchPmDisableEnergyReport

Offset 0x0A2E - PCH Pm Disable Energy Report Disable/Enable PCH to CPU energy report feature.

\$EN\_DIS

Definition at line 2969 of file FspUpd.h.

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**8.7.2.47** `UINT8 FSP_S_TEST_CONFIG::PchSbAccessUnlock`

Offset 0x0893 - PCH Psf lock bit The PSF registers will be locked before 3rd party code execution.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line 2891 of file FspUpd.h.

**8.7.2.48** `UINT8 FSP_S_TEST_CONFIG::PchSbiUnlock`

Offset 0x0892 - PCH Sbi lock bit This unlock the SBI lock bit to allow SBI after post time.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line 2885 of file FspUpd.h.

**8.7.2.49** `UINT8 FSP_S_TEST_CONFIG::PcieEnablePort8xhDecode`

Offset 0x0A2C - PCIE RP Enable Port8xh Decode This member describes whether PCIE root port Port 8xh Decode is enabled.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line 2958 of file FspUpd.h.

**8.7.2.50** `UINT8 FSP_S_TEST_CONFIG::PcieRpDptp[24]`

Offset 0x0A14 - PCIE RP Downstream Port Transmitter Preset Used during Gen3 Link Equalization.

Used for all lanes. Default is 7.

Definition at line 2951 of file FspUpd.h.

**8.7.2.51** `UINT8 FSP_S_TEST_CONFIG::PcieRpSlotPowerLimitScale[24]`

Offset 0x09B4 - PCIE RP Slot Power Limit Scale Specifies scale used for slot power limit value.

Leave as 0 to set to default.

Definition at line 2936 of file FspUpd.h.

**8.7.2.52** `UINT16 FSP_S_TEST_CONFIG::PcieRpSlotPowerLimitValue[24]`

Offset 0x09CC - PCIE RP Slot Power Limit Value Specifies upper limit on power supply by slot.

Leave as 0 to set to default.

Definition at line 2941 of file FspUpd.h.

**8.7.2.53** `UINT8 FSP_S_TEST_CONFIG::PcieRpUptp[24]`

Offset 0x09FC - PCIE RP Upstream Port Transmitter Preset Used during Gen3 Link Equalization.

Used for all lanes. Default is 5.

Definition at line 2946 of file FspUpd.h.

**8.7.2.54** `UINT8 FSP_S_TEST_CONFIG::PkgCStateDemotion`

Offset 0x07DA - Enable or Disable Package C-State Demotion Enable or Disable Package C-State Demotion.

---

0: Disable; 1: Enable; **2: Auto** (Auto: Enabled for Skylake; Disabled for Kabylake) 0:Disable, 1:Enable, 2:Auto  
Definition at line 2566 of file FspsUpd.h.

#### 8.7.2.55 UINT8 FSP\_S\_TEST\_CONFIG::PkgCStateLimit

Offset 0x07DF - Set the Max Pkg Cstate Set the Max Pkg Cstate.

Default set to Auto which limits the Max Pkg Cstate to deep C-state. Valid values 0 - C0/C1 , 1 - C2 , 2 - C3 , 3 - C6 , 4 - C7 , 5 - C7S , 6 - C8 , 7 - C9 , 8 - C10 , 254 - CPU Default , 255 - Auto

Definition at line 2598 of file FspsUpd.h.

#### 8.7.2.56 UINT8 FSP\_S\_TEST\_CONFIG::PkgCStateUnDemotion

Offset 0x07DB - Enable or Disable Package C-State UnDemotion Enable or Disable Package C-State UnDemotion.

0: Disable; 1: Enable; **2: Auto** (Auto: Enabled for Skylake; Disabled for Kabylake) 0:Disable, 1:Enable, 2:Auto

Definition at line 2573 of file FspsUpd.h.

#### 8.7.2.57 UINT8 FSP\_S\_TEST\_CONFIG::PmgCstCfgCtrlLock

Offset 0x07D8 - Configure C-State Configuration Lock Configure C-State Configuration Lock; 0: Disable; **1: Enable.**  
\$EN\_DIS

Definition at line 2553 of file FspsUpd.h.

#### 8.7.2.58 UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit1

Offset 0x0848 - Package Long duration turbo mode power limit Package Long duration turbo mode power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit. Valid Range 0 to 4095875 in Step size of 125

Definition at line 2711 of file FspsUpd.h.

#### 8.7.2.59 UINT8 FSP\_S\_TEST\_CONFIG::PowerLimit1Time

Offset 0x07A3 - Package Long duration turbo mode time Package Long duration turbo mode time window in seconds.

Valid values(Unit in seconds) 0 to 8 , 10 , 12 , 14 , 16 , 20 , 24 , 28 , 32 , 40 , 48 , 56 , 64 , 80 , 96 , 112 , 128

Definition at line 2250 of file FspsUpd.h.

#### 8.7.2.60 UINT8 FSP\_S\_TEST\_CONFIG::PowerLimit2

Offset 0x07A4 - Short Duration Turbo Mode Enable or Disable short duration Turbo Mode.

0 : Disable; **1: Enable** \$EN\_DIS

Definition at line 2256 of file FspsUpd.h.

#### 8.7.2.61 UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit2Power

Offset 0x084C - Package Short duration turbo mode power limit Package Short duration turbo mode power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2717 of file FspsUpd.h.

**8.7.2.62 UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit3**

Offset 0x0850 - Package PL3 power limit Package PL3 power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2723 of file FspUpd.h.

**8.7.2.63 UINT8 FSP\_S\_TEST\_CONFIG::PowerLimit3Time**

Offset 0x07A6 - Package PL3 time window Package PL3 time window range for this policy in milliseconds.

Valid values are 0, 3 to 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 55, 56, 64

Definition at line 2268 of file FspUpd.h.

**8.7.2.64 UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit4**

Offset 0x0854 - Package PL4 power limit Package PL4 power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2729 of file FspUpd.h.

**8.7.2.65 UINT8 FSP\_S\_TEST\_CONFIG::ProcHotResponse**

Offset 0x07D3 - Enable or Disable PROCHOT# Response Enable or Disable PROCHOT# Response; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2523 of file FspUpd.h.

**8.7.2.66 UINT8 FSP\_S\_TEST\_CONFIG::ProcTraceEnable**

Offset 0x07C9 - Enable or Disable Processor Trace feature Enable or Disable Processor Trace feature; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2458 of file FspUpd.h.

**8.7.2.67 UINT8 FSP\_S\_TEST\_CONFIG::ProcTraceOutputScheme**

Offset 0x07C8 - Control on Processor Trace output scheme Control on Processor Trace output scheme; **0: Single Range Output**; 1: ToPA Output.

0:Single Range Output, 1:ToPA Output

Definition at line 2452 of file FspUpd.h.

**8.7.2.68 UINT16 FSP\_S\_TEST\_CONFIG::PsysPmax**

Offset 0x087C - Platform Power Pmax PCODE MMIO Mailbox: Platform Power Pmax.

**0 - Auto** Specified in 1/8 Watt increments. Range 0-1024 Watts. Value of 800 = 100W

Definition at line 2789 of file FspUpd.h.

#### 8.7.2.69 UINT8 FSP\_S\_TEST\_CONFIG::PsysPowerLimit1

Offset 0x07B9 - PL1 Enable value PL1 Enable value to limit average platform power.

**0: Disable**; 1: Enable. \$EN\_DIS

Definition at line 2377 of file FspsUpd.h.

#### 8.7.2.70 UINT32 FSP\_S\_TEST\_CONFIG::PsysPowerLimit1Power

Offset 0x0874 - Platform PL1 power Platform PL1 power.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2777 of file FspsUpd.h.

#### 8.7.2.71 UINT8 FSP\_S\_TEST\_CONFIG::PsysPowerLimit2

Offset 0x07BB - PL2 Enable Value PL2 Enable activates the PL2 value to limit average platform power.

**0: Disable**; 1: Enable. \$EN\_DIS

Definition at line 2390 of file FspsUpd.h.

#### 8.7.2.72 UINT32 FSP\_S\_TEST\_CONFIG::PsysPowerLimit2Power

Offset 0x0878 - Platform PL2 power Platform PL2 power.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line 2783 of file FspsUpd.h.

#### 8.7.2.73 UINT8 FSP\_S\_TEST\_CONFIG::RaceToHalt

Offset 0x07E9 - Race To Halt Enable/Disable Race To Halt feature.

RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)Disable; **1: Enable** \$EN\_DIS

Definition at line 2661 of file FspsUpd.h.

#### 8.7.2.74 UINT8 FSP\_S\_TEST\_CONFIG::SataTestMode

Offset 0x0A30 - PCH Sata Test Mode Allow entrance to the PCH SATA test modes.

\$EN\_DIS

Definition at line 2981 of file FspsUpd.h.

#### 8.7.2.75 UINT8 FSP\_S\_TEST\_CONFIG::SevenCoreRatioLimit

Offset 0x0886 - 7-Core Ratio Limit 7-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 7-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.Range is 0 to 255

Definition at line 2817 of file FspsUpd.h.

#### 8.7.2.76 UINT8 FSP\_S\_TEST\_CONFIG::SixCoreRatioLimit

Offset 0x0885 - 6-Core Ratio Limit 6-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.



This 6-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2811 of file FspUpd.h.

#### 8.7.2.77 UINT16 FSP\_S\_TEST\_CONFIG::StateRatio[40]

Offset 0x07EC - Maximum P-state ratio to use in the custom P-state table Maximum P-state ratio to use in the custom P-state table.

NumOfCustomPStates has valid range between 0 to 40. For no. of P-States supported(NumOfCustomPStates) , StateRatio[NumOfCustomPStates] are configurable. Valid Range of value is 0 to 0x7F

Definition at line 2673 of file FspUpd.h.

#### 8.7.2.78 UINT8 FSP\_S\_TEST\_CONFIG::TccActivationOffset

Offset 0x07AA - TCC Activation Offset TCC Activation Offset.

Offset from factory set TCC activation temperature at which the Thermal Control Circuit must be activated. TCC will be activated at TCC Activation Temperature, in volts. For SKL Y SKU, the recommended default for this policy is **10**, For all other SKUs the recommended default are **0**

Definition at line 2293 of file FspUpd.h.

#### 8.7.2.79 UINT8 FSP\_S\_TEST\_CONFIG::TccOffsetClamp

Offset 0x07AB - Tcc Offset Clamp Enable/Disable Tcc Offset Clamp for Runtime Average Temperature Limit (RATL) allows CPU to throttle below P1. For SKL Y SKU, the recommended default for this policy is **1: Enabled**, For all other SKUs the recommended default are **0: Disabled**.

\$EN\_DIS

Definition at line 2301 of file FspUpd.h.

#### 8.7.2.80 UINT8 FSP\_S\_TEST\_CONFIG::TccOffsetLock

Offset 0x07AC - Tcc Offset Lock Tcc Offset Lock for Runtime Average Temperature Limit (RATL) to lock temperature target; **0: Disabled**; 1: Enabled.

\$EN\_DIS

Definition at line 2308 of file FspUpd.h.

#### 8.7.2.81 UINT32 FSP\_S\_TEST\_CONFIG::TccOffsetTimeWindowForRatl

Offset 0x0858 - Tcc Offset Time Window for RATL Package PL4 power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit. Valid Range 0 to 4095875 in Step size of 125

Definition at line 2735 of file FspUpd.h.

#### 8.7.2.82 UINT8 FSP\_S\_TEST\_CONFIG::ThreeCoreRatioLimit

Offset 0x079E - 3-Core Ratio Limit 3-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 3-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2221 of file FspUpd.h.

### 8.7.2.83 UINT8 FSP\_S\_TEST\_CONFIG::ThreeStrikeCounterDisable

Offset 0x0888 - Set Three Strike Counter Disable False (default): Three Strike counter will be incremented and True: Prevents Three Strike counter from incrementing; **0: False**; 1: True.

0: False, 1: True

Definition at line 2830 of file FspUpd.h.

### 8.7.2.84 UINT8 FSP\_S\_TEST\_CONFIG::TimedMwait

Offset 0x07DD - Enable or Disable TimedMwait Support.

Enable or Disable TimedMwait Support. **0: Disable**; 1: Enable \$EN\_DIS

Definition at line 2585 of file FspUpd.h.

### 8.7.2.85 UINT8 FSP\_S\_TEST\_CONFIG::TStates

Offset 0x07D0 - Enable or Disable T states Enable or Disable T states; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line 2505 of file FspUpd.h.

### 8.7.2.86 UINT8 FSP\_S\_TEST\_CONFIG::TwoCoreRatioLimit

Offset 0x079D - 2-Core Ratio Limit 2-Core Ratio Limit: LFM to Fused max, For overclocking part: LFM to 255.

This 2-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line 2215 of file FspUpd.h.

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)

## 8.8 FSP\_T\_CONFIG Struct Reference

Fsp T Configuration.

```
#include <FsptUpd.h>
```

### Public Attributes

- UINT8 [PcdSerialIoUartDebugEnabled](#)  
*Offset 0x0040 - PcdSerialIoUartDebugEnabled Enable SerialIo Uart debug library with/without initializing SerialIo Uart device in FSP.*
- UINT8 [PcdSerialIoUartNumber](#)  
*Offset 0x0041 - PcdSerialIoUartNumber Select SerialIo Uart Controller for debug.*
- UINT8 [UnusedUpdSpace0](#) [2]  
*Offset 0x0042.*
- UINT32 [PcdSerialIoUartInputClock](#)  
*Offset 0x0044.*
- UINT64 [PcdPciExpressBaseAddress](#)  
*Offset 0x0048 - Pci Express Base Address Base address to be programmed for Pci Express.*
- UINT32 [PcdPciExpressRegionLength](#)

Offset 0x0050 - Pci Express Region Length Region Length to be programmed for Pci Express.

- [UINT8 ReservedFsptUpd1](#) [12]

Offset 0x0054.

### 8.8.1 Detailed Description

Fsp T Configuration.

Definition at line 69 of file FsptUpd.h.

### 8.8.2 Member Data Documentation

#### 8.8.2.1 UINT8 FSP\_T\_CONFIG::PcdSerialloUartDebugEnabled

Offset 0x0040 - PcdSerialloUartDebugEnabled Enable Seriallo Uart debug library with/without initializing Seriallo Uart device in FSP.

0:Disable, 1:Enable and Initialize, 2:Enable without Initializing

Definition at line 75 of file FsptUpd.h.

#### 8.8.2.2 UINT8 FSP\_T\_CONFIG::PcdSerialloUartNumber

Offset 0x0041 - PcdSerialloUartNumber Select Seriallo Uart Controller for debug.

0:SerialloUart0, 1:SerialloUart1, 2:SerialloUart2

Definition at line 81 of file FsptUpd.h.

The documentation for this struct was generated from the following file:

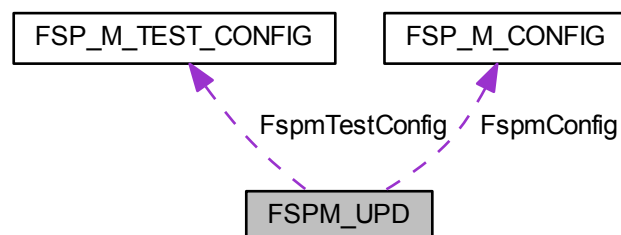
- [FsptUpd.h](#)

## 8.9 FSPM\_UPD Struct Reference

Fsp M UPD Configuration.

```
#include <FspmUpd.h>
```

Collaboration diagram for FSPM\_UPD:



## Public Attributes

- FSP\_UPD\_HEADER [FspUpdHeader](#)  
*Offset 0x0000.*
- FSPM\_ARCH\_UPD [FspmArchUpd](#)  
*Offset 0x0020.*
- FSP\_M\_CONFIG [FspmConfig](#)  
*Offset 0x0040.*
- FSP\_M\_TEST\_CONFIG [FspmTestConfig](#)  
*Offset 0x0520.*
- UINT8 [UnusedUpdSpace10](#) [134]  
*Offset 0x05C0.*
- UINT16 [UpdTerminator](#)  
*Offset 0x0646.*

### 8.9.1 Detailed Description

Fsp M UPD Configuration.

Definition at line 1693 of file FspmUpd.h.

The documentation for this struct was generated from the following file:

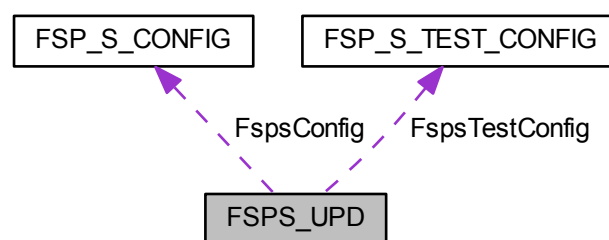
- [FspmUpd.h](#)

## 8.10 FSPS\_UPD Struct Reference

Fsp S UPD Configuration.

```
#include <FspsUpd.h>
```

Collaboration diagram for FSPS\_UPD:



## Public Attributes

- FSP\_UPD\_HEADER [FspUpdHeader](#)  
*Offset 0x0000.*
- FSP\_S\_CONFIG [FspsConfig](#)  
*Offset 0x0020.*

- [FSP\\_S\\_TEST\\_CONFIG](#) [FspTestConfig](#)  
*Offset 0x0780.*
- UINT8 [UnusedUpdSpace26](#) [470]  
*Offset 0x0A40.*
- UINT16 [UpdTerminator](#)  
*Offset 0x0C16.*

### 8.10.1 Detailed Description

Fsp S UPD Configuration.

Definition at line 2990 of file [FspUpd.h](#).

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)

## 8.11 FSPT\_CORE\_UPD Struct Reference

Fsp T Core UPD.

```
#include <FsptUpd.h>
```

### Public Attributes

- UINT32 [MicrocodeRegionBase](#)  
*Offset 0x0020.*
- UINT32 [MicrocodeRegionSize](#)  
*Offset 0x0024.*
- UINT32 [CodeRegionBase](#)  
*Offset 0x0028.*
- UINT32 [CodeRegionSize](#)  
*Offset 0x002C.*
- UINT8 [Reserved](#) [16]  
*Offset 0x0030.*

### 8.11.1 Detailed Description

Fsp T Core UPD.

Definition at line 44 of file [FsptUpd.h](#).

The documentation for this struct was generated from the following file:

- [FsptUpd.h](#)

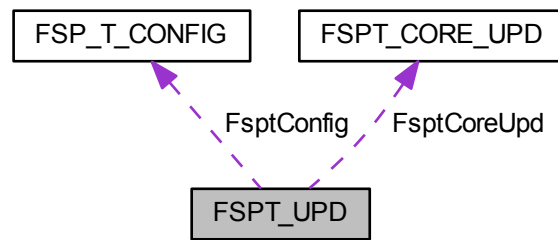
## 8.12 FSPT\_UPD Struct Reference

Fsp T UPD Configuration.

```
#include <FsptUpd.h>
```

---

Collaboration diagram for FSPT\_UPD:



### Public Attributes

- FSP\_UPD\_HEADER [FspUpdHeader](#)  
*Offset 0x0000.*
- FSPT\_CORE\_UPD [FsptCoreUpd](#)  
*Offset 0x0020.*
- FSP\_T\_CONFIG [FsptConfig](#)  
*Offset 0x0040.*
- UINT8 [UnusedUpdSpace1](#) [6]  
*Offset 0x0060.*
- UINT16 [UpdTerminator](#)  
*Offset 0x0066.*

#### 8.12.1 Detailed Description

Fsp T UPD Configuration.

Definition at line 108 of file `FsptUpd.h`.

The documentation for this struct was generated from the following file:

- [FsptUpd.h](#)

### 8.13 GPIO\_CONFIG Struct Reference

GPIO configuration structure used for pin programming.

```
#include <GpioConfig.h>
```

### Public Attributes

- UINT32 [PadMode](#): 5  
*Pad Mode Pad can be set as GPIO or one of its native functions.*
- UINT32 [HostSoftPadOwn](#): 2  
*Host Software Pad Ownership Set pad to ACPI mode or GPIO Driver Mode.*

- UIN32 [Direction](#): 6  
*GPIO Direction Can choose between In, In with inversion, Out, both In and Out, both In with inversion and out or disabling both.*
- UIN32 [OutputState](#): 2  
*Output State Set Pad output value.*
- UIN32 [InterruptConfig](#): 9  
*GPIO Interrupt Configuration Set Pad to cause one of interrupts (IOxAPIC/SCI/SMI/NMI).*
- UIN32 [PowerConfig](#): 8  
*GPIO Power Configuration.*
- UIN32 [ElectricalConfig](#): 9  
*GPIO Electrical Configuration This setting controls pads termination and voltage tolerance.*
- UIN32 [LockConfig](#): 4  
*GPIO Lock Configuration This setting controls pads lock.*
- UIN32 [OtherSettings](#): 2  
*Additional GPIO configuration Refer to definition of GPIO\_OTHER\_CONFIG for supported settings.*
- UIN32 [RsvdBits](#): 17  
*Reserved bits for future extension.*

### 8.13.1 Detailed Description

GPIO configuration structure used for pin programming.

Structure contains fields that can be used to configure pad.

Definition at line 55 of file GpioConfig.h.

### 8.13.2 Member Data Documentation

#### 8.13.2.1 UIN32 GPIO\_CONFIG::Direction

GPIO Direction Can choose between In, In with inversion, Out, both In and Out, both In with inversion and out or disabling both.

Refer to definition of GPIO\_DIRECTION for supported settings.

Definition at line 76 of file GpioConfig.h.

#### 8.13.2.2 UIN32 GPIO\_CONFIG::ElectricalConfig

GPIO Electrical Configuration This setting controls pads termination and voltage tolerance.

Refer to definition of GPIO\_ELECTRICAL\_CONFIG for supported settings.

Definition at line 102 of file GpioConfig.h.

#### 8.13.2.3 UIN32 GPIO\_CONFIG::HostSoftPadOwn

Host Software Pad Ownership Set pad to ACPI mode or GPIO Driver Mode.

Refer to definition of GPIO\_HOSTSW\_OWN.

Definition at line 70 of file GpioConfig.h.

---

#### 8.13.2.4 UINT32 GPIO\_CONFIG::InterruptConfig

GPIO Interrupt Configuration Set Pad to cause one of interrupts (IOxAPIC/SCI/SMI/NMI).

This setting is applicable only if GPIO is in GpioMode with input enabled. Refer to definition of GPIO\_INT\_CONFIG for supported settings.

Definition at line 90 of file GpioConfig.h.

#### 8.13.2.5 UINT32 GPIO\_CONFIG::LockConfig

GPIO Lock Configuration This setting controls pads lock.

Refer to definition of GPIO\_LOCK\_CONFIG for supported settings.

Definition at line 108 of file GpioConfig.h.

#### 8.13.2.6 UINT32 GPIO\_CONFIG::OutputState

Output State Set Pad output value.

Refer to definition of GPIO\_OUTPUT\_STATE for supported settings. This setting takes place when output is enabled.

Definition at line 83 of file GpioConfig.h.

#### 8.13.2.7 UINT32 GPIO\_CONFIG::PadMode

Pad Mode Pad can be set as GPIO or one of its native functions.

When in native mode setting Direction (except Inversion), OutputState, InterruptConfig, Host Software Pad Ownership and OutputStateLock are unnecessary. Refer to definition of GPIO\_PAD\_MODE. Refer to EDS for each native mode according to the pad.

Definition at line 64 of file GpioConfig.h.

#### 8.13.2.8 UINT32 GPIO\_CONFIG::PowerConfig

GPIO Power Configuration.

This setting controls Pad Reset Configuration. Refer to definition of GPIO\_RESET\_CONFIG for supported settings.

Definition at line 96 of file GpioConfig.h.

The documentation for this struct was generated from the following file:

- [GpioConfig.h](#)

## 8.14 MEMORY\_PLATFORM\_DATA Struct Reference

Memory Platform Data Hob.

```
#include <MemInfoHob.h>
```

### 8.14.1 Detailed Description

Memory Platform Data Hob.

**Revision 1:**

---



- Initial version. **Revision 2:**
- Added TsegBase, PrmrrSize, PrmrrBase, Gttbase, MmioSize, PciEBaseAddress fields

Definition at line 259 of file MemInfoHob.h.

The documentation for this struct was generated from the following file:

- [MemInfoHob.h](#)

## 8.15 SI\_CHIPSET\_INIT\_INFO Struct Reference

The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC.

```
#include <FspmUpd.h>
```

### 8.15.1 Detailed Description

The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC.

Definition at line 47 of file FspmUpd.h.

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)

## 8.16 SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG Struct Reference

The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device.

```
#include <FspsUpd.h>
```

### Public Attributes

- UINT8 [Device](#)  
*Device number.*
- UINT8 [Function](#)  
*Device function.*
- UINT8 [IntX](#)  
*Interrupt pin: INTA-INTD (see SI\_PCH\_INT\_PIN)*
- UINT8 [Irq](#)  
*IRQ to be set for device.*

### 8.16.1 Detailed Description

The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device.

Definition at line 76 of file FspsUpd.h.

The documentation for this struct was generated from the following file:

- [FspsUpd.h](#)
-

## 8.17 SMBIOS\_CACHE\_INFO Struct Reference

SMBIOS Cache Info HOB Structure.

```
#include <SmbiosCacheInfoHob.h>
```

### Public Attributes

- UINT16 [NumberOfCacheLevels](#)  
*Based on Number of Cache Types L1/L2/L3.*
- UINT8 [SocketDesignationStrIndex](#)  
*String Index in the string Buffer. Example "L1-CACHE".*
- UINT16 [CacheConfiguration](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.8 Table 36.*
- UINT16 [MaxCacheSize](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.8.1.*
- UINT16 [InstalledSize](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.8.1.*
- UINT16 [SupportedSramType](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.8.2.*
- UINT16 [CurrentSramType](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.8.2.*
- UINT8 [CacheSpeed](#)  
*Cache Speed in nanoseconds. 0 if speed is unknown.*
- UINT8 [ErrorCorrectionType](#)  
*ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.3.*
- UINT8 [SystemCacheType](#)  
*ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.4.*
- UINT8 [Associativity](#)  
*ENUM Format defined in SMBIOS Spec v3.0 Section 7.8.5.*

### 8.17.1 Detailed Description

SMBIOS Cache Info HOB Structure.

Definition at line 32 of file `SmbiosCacheInfoHob.h`.

The documentation for this struct was generated from the following file:

- [SmbiosCacheInfoHob.h](#)

## 8.18 SMBIOS\_PROCESSOR\_INFO Struct Reference

SMBIOS Processor Info HOB Structure.

```
#include <SmbiosProcessorInfoHob.h>
```

---

## Public Attributes

- [UINT8 ProcessorType](#)  
*ENUM defined in SMBIOS Spec v3.0 Section 7.5.1.*
- [UINT16 ProcessorFamily](#)  
*This info is used for both ProcessorFamily and ProcessorFamily2 fields See ENUM defined in SMBIOS Spec v3.0 Section 7.5.2.*
- [UINT8 ProcessorManufacturerStrIndex](#)  
*Index of the String in the String Buffer.*
- [UINT64 ProcessorId](#)  
*ENUM defined in SMBIOS Spec v3.0 Section 7.5.3.*
- [UINT8 ProcessorVersionStrIndex](#)  
*Index of the String in the String Buffer.*
- [UINT8 Voltage](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.5.4.*
- [UINT16 ExternalClockInMHz](#)  
*External Clock Frequency. Set to 0 if unknown.*
- [UINT16 CurrentSpeedInMHz](#)  
*Snapshot of current processor speed during boot.*
- [UINT8 Status](#)  
*Format defined in the SMBIOS Spec v3.0 Table 21.*
- [UINT8 ProcessorUpgrade](#)  
*ENUM defined in SMBIOS Spec v3.0 Section 7.5.5.*
- [UINT16 CoreCount](#)  
*This info is used for both CoreCount & CoreCount2 fields See detailed description in SMBIOS Spec v3.0 Section 7.5.6.*
- [UINT16 EnabledCoreCount](#)  
*This info is used for both CoreEnabled & CoreEnabled2 fields See detailed description in SMBIOS Spec v3.0 Section 7.5.7.*
- [UINT16 ThreadCount](#)  
*This info is used for both ThreadCount & ThreadCount2 fields See detailed description in SMBIOS Spec v3.0 Section 7.5.8.*
- [UINT16 ProcessorCharacteristics](#)  
*Format defined in SMBIOS Spec v3.0 Section 7.5.9.*

### 8.18.1 Detailed Description

SMBIOS Processor Info HOB Structure.

Definition at line 32 of file SmbiosProcessorInfoHob.h.

The documentation for this struct was generated from the following file:

- [SmbiosProcessorInfoHob.h](#)



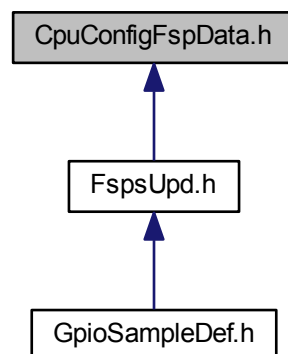
## Chapter 9

# File Documentation

### 9.1 CpuConfigFspData.h File Reference

FSP CPU Data Config Block.

This graph shows which files directly or indirectly include this file:



#### 9.1.1 Detailed Description

FSP CPU Data Config Block.

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#### Specification Reference:

## 9.2 DoxygenFspIntegrationGuide.h File Reference

This file contains doxygen KabylakeFspIntegration Guide.

### 9.2.1 Detailed Description

This file contains doxygen KabylakeFspIntegration Guide.

#### Copyright

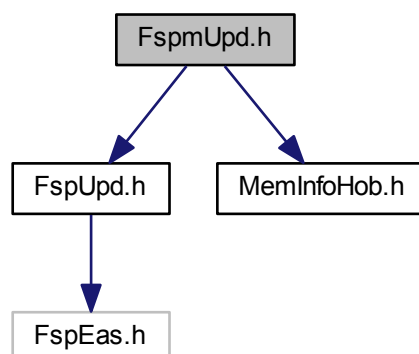
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## 9.3 FspmUpd.h File Reference

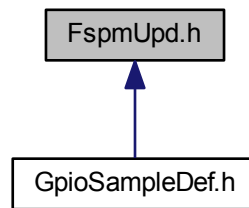
```
#include <FspUpd.h>
```

```
#include <MemInfoHob.h>
```

Include dependency graph for FspmUpd.h:



This graph shows which files directly or indirectly include this file:



## Classes

- struct [SI\\_CHIPSET\\_INIT\\_INFO](#)  
*The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC.*
- struct [FSP\\_M\\_CONFIG](#)  
*Fsp M Configuration.*
- struct [FSP\\_M\\_TEST\\_CONFIG](#)  
*Fsp M Test Configuration.*
- struct [FSPM\\_UPD](#)  
*Fsp M UPD Configuration.*

### 9.3.1 Detailed Description

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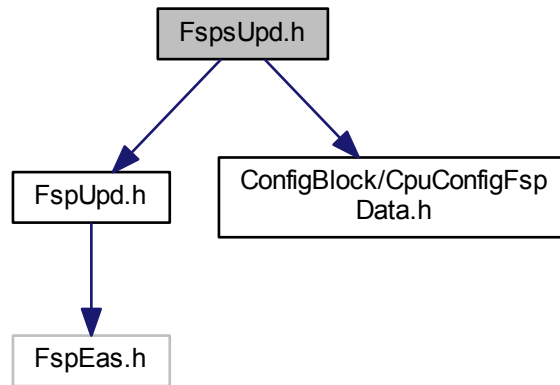
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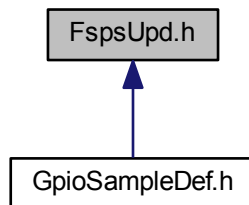
## 9.4 FspUpd.h File Reference

```
#include <FspUpd.h>
#include <ConfigBlock/CpuConfigFspData.h>
```

Include dependency graph for FspUpd.h:



This graph shows which files directly or indirectly include this file:



### Classes

- struct [AZALIA\\_HEADER](#)  
*Azalia Header structure.*
- struct [AUDIO\\_AZALIA\\_VERB\\_TABLE](#)  
*Audio Azalia Verb Table structure.*
- struct [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)  
*The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device.*
- struct [FSP\\_S\\_CONFIG](#)  
*Fsp S Configuration.*
- struct [FSP\\_S\\_TEST\\_CONFIG](#)  
*Fsp S Test Configuration.*



- struct [FSPS\\_UPD](#)

*Fsp S UPD Configuration.*

## Macros

- #define [SI\\_PCH\\_MAX\\_DEVICE\\_INTERRUPT\\_CONFIG](#) 64

*Number of all PCH devices.*

## Enumerations

- enum [SI\\_PCH\\_INT\\_PIN](#)

*Refer to the definition of PCH\_INT\_PIN.*

### 9.4.1 Detailed Description

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### 9.4.2 Enumeration Type Documentation

#### 9.4.2.1 enum [SI\\_PCH\\_INT\\_PIN](#)

Refer to the definition of PCH\_INT\_PIN.

#### Enumerator

***SiPchNoInt*** No Interrupt Pin.

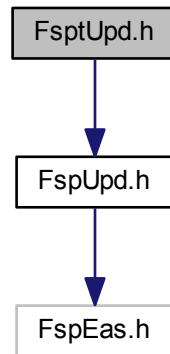
Definition at line 66 of file FspSUpd.h.

---

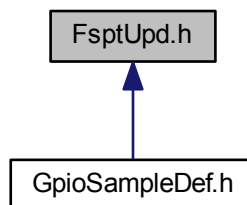
## 9.5 FsptUpd.h File Reference

```
#include <FsptUpd.h>
```

Include dependency graph for FsptUpd.h:



This graph shows which files directly or indirectly include this file:



### Classes

- struct [FSPT\\_CORE\\_UPD](#)  
*Fsp T Core UPD.*
- struct [FSP\\_T\\_CONFIG](#)  
*Fsp T Configuration.*
- struct [FSPT\\_UPD](#)  
*Fsp T UPD Configuration.*

#### 9.5.1 Detailed Description

---

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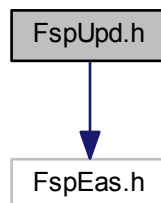
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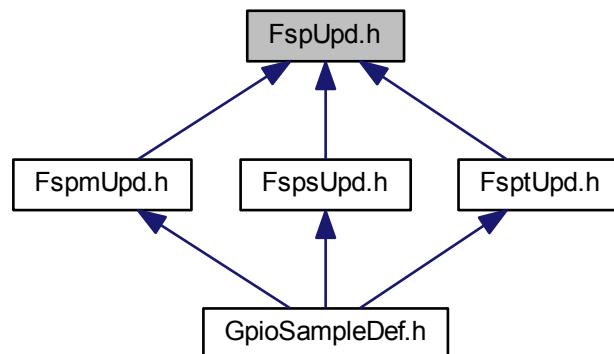
## 9.6 FspUpd.h File Reference

```
#include <FspEas.h>
```

Include dependency graph for FspUpd.h:



This graph shows which files directly or indirectly include this file:



### 9.6.1 Detailed Description

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## 9.7 GpioConfig.h File Reference

Header file for GpioConfig structure used by GPIO library.

#### Classes

- struct [GPIO\\_CONFIG](#)

*GPIO configuration structure used for pin programming.*

## Macros

- #define [B\\_GPIO\\_INT\\_CONFIG\\_INT\\_SOURCE\\_MASK](#) 0x1F  
*Mask for GPIO\_INT\_CONFIG for interrupt source.*
- #define [B\\_GPIO\\_INT\\_CONFIG\\_INT\\_TYPE\\_MASK](#) 0xE0  
*Mask for GPIO\_INT\_CONFIG for interrupt type.*
- #define [B\\_GPIO\\_ELECTRICAL\\_CONFIG\\_TERMINATION\\_MASK](#) 0x1F  
*Mask for GPIO\_ELECTRICAL\_CONFIG for termination value.*
- #define [B\\_GPIO\\_ELECTRICAL\\_CONFIG\\_1V8\\_TOLERANCE\\_MASK](#) 0x60  
*Mask for GPIO\_ELECTRICAL\_CONFIG for 1v8 tolerance setting.*
- #define [B\\_GPIO\\_LOCK\\_CONFIG\\_PAD\\_CONF\\_LOCK\\_MASK](#) 0x3  
*Mask for GPIO\_LOCK\_CONFIG for Pad Configuration Lock.*
- #define [B\\_GPIO\\_LOCK\\_CONFIG\\_OUTPUT\\_LOCK\\_MASK](#) 0x5  
*Mask for GPIO\_LOCK\_CONFIG for Pad Output Lock.*
- #define [B\\_GPIO\\_OTHER\\_CONFIG\\_RXRAW\\_MASK](#) 0x3  
*Mask for GPIO\_OTHER\_CONFIG for RxRaw1 setting.*

## Typedefs

- typedef UINT32 [GPIO\\_PAD](#)  
*For any GpioPad usage in code use GPIO\_PAD type.*
- typedef UINT32 [GPIO\\_GROUP](#)  
*For any GpioGroup usage in code use GPIO\_GROUP type.*

## Enumerations

- enum [GPIO\\_HARDWARE\\_DEFAULT](#)
- enum [GPIO\\_PAD\\_MODE](#)  
*GPIO Pad Mode Refer to GPIO documentation on native functions available for certain pad.*
- enum [GPIO\\_HOSTSW\\_OWN](#)  
*Host Software Pad Ownership modes This setting affects GPIO interrupt status registers.*
- enum [GPIO\\_DIRECTION](#)  
*GPIO Direction.*
- enum [GPIO\\_OUTPUT\\_STATE](#)  
*GPIO Output State This field is relevant only if output is enabled.*
- enum [GPIO\\_INT\\_CONFIG](#)  
*GPIO interrupt configuration This setting is applicable only if pad is in GPIO mode and has input enabled.*
- enum [GPIO\\_RESET\\_CONFIG](#)  
*GPIO Power Configuration GPIO\_RESET\_CONFIG allows to set GPIO Reset type (PADCFG\_DW0.PadRstCfg) which will be used to reset certain GPIO settings.*
- enum [GPIO\\_ELECTRICAL\\_CONFIG](#)  
*GPIO Electrical Configuration Set GPIO termination and Pad Tolerance (applicable only for some pads) Field from GpioTermNone to GpioTermNative can be OR'ed with GpioTolerance1v8.*
- enum [GPIO\\_LOCK\\_CONFIG](#)  
*GPIO LockConfiguration Set GPIO configuration lock and output state lock.*
- enum [GPIO\\_OTHER\\_CONFIG](#)  
*Other GPIO Configuration GPIO\_OTHER\_CONFIG is used for less often settings and for future extensions Supported settings:*

### 9.7.1 Detailed Description

Header file for GpioConfig structure used by GPIO library.

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#### Specification Reference:

### 9.7.2 Enumeration Type Documentation

#### 9.7.2.1 enum GPIO\_DIRECTION

GPIO Direction.

##### Enumerator

- GpioDirDefault** Leave pad direction setting unmodified.
- GpioDirInOut** Set pad for both output and input.
- GpioDirInOutInv** Set pad for both output and input with inversion.
- GpioDirIn** Set pad for input only.
- GpioDirInInv** Set pad for input with inversion.
- GpioDirOut** Set pad for output only.
- GpioDirNone** Disable both output and input.

Definition at line 167 of file GpioConfig.h.

#### 9.7.2.2 enum GPIO\_ELECTRICAL\_CONFIG

GPIO Electrical Configuration Set GPIO termination and Pad Tolerance (applicable only for some pads) Field from GpioTermNone to GpioTermNative can be OR'ed with GpioTolerance1v8.

##### Enumerator

- GpioTermDefault** Leave termination setting unmodified.
- GpioTermNone** none

**GpioTermWpd5K** 5kOhm weak pull-down  
**GpioTermWpd20K** 20kOhm weak pull-down  
**GpioTermWpu1K** 1kOhm weak pull-up  
**GpioTermWpu2K** 2kOhm weak pull-up  
**GpioTermWpu5K** 5kOhm weak pull-up  
**GpioTermWpu20K** 20kOhm weak pull-up  
**GpioTermWpu1K2K** 1kOhm & 2kOhm weak pull-up  
**GpioTermNative** Native function controls pads termination This setting is applicable only to some native modes. Please check EDS to determine which native functionality can control pads termination  
**GpioNoTolerance1v8** Disable 1.8V pad tolerance.  
**GpioTolerance1v8** Enable 1.8V pad tolerance.

Definition at line 296 of file GpioConfig.h.

#### 9.7.2.3 enum GPIO\_HARDWARE\_DEFAULT

Enumerator

**GpioHardwareDefault** Leave setting unmodified.

Definition at line 118 of file GpioConfig.h.

#### 9.7.2.4 enum GPIO\_HOSTSW\_OWN

Host Software Pad Ownership modes This setting affects GPIO interrupt status registers.

Depending on chosen ownership some GPIO Interrupt status register get updated and other masked. Please refer to EDS for HOSTSW\_OWN register description.

Enumerator

**GpioHostOwnDefault** Leave ownership value unmodified.

**GpioHostOwnAcpi** Set HOST ownership to ACPI. Use this setting if pad is not going to be used by GPIO OS driver. If GPIO is configured to generate SCI/SMI/NMI then this setting must be used for interrupts to work

**GpioHostOwnGpio** Set HOST ownership to GPIO Driver mode. Use this setting only if GPIO pad should be controlled by GPIO OS Driver. GPIO OS Driver will be able to control the pad if appropriate entry in ACPI exists (refer to ACPI specification for Gpiolo and GpioInt descriptors)

Definition at line 146 of file GpioConfig.h.

#### 9.7.2.5 enum GPIO\_INT\_CONFIG

GPIO interrupt configuration This setting is applicable only if pad is in GPIO mode and has input enabled.

GPIO\_INT\_CONFIG allows to choose which interrupt is generated (IOxAPIC/SCI/SMI/NMI) and how it is triggered (edge or level). Refer to PADCFG\_DW0 register description in EDS for details on this settings. Field from GpioIntNmi to GpioIntApic can be OR'ed with GpioIntLevel to GpioIntBothEdge to describe an interrupt e.g. GpioIntApic | GpioIntLevel If GPIO is set to cause an SCI then also GPI\_GPE\_EN is enabled for this pad. If GPIO is set to cause an NMI then also GPI\_NMI\_EN is enabled for this pad. Not all GPIO are capable of generating an SMI or NMI interrupt. When routing GPIO to cause an IOxAPIC interrupt care must be taken, as this interrupt cannot be shared and its IRQn number is not configurable. Refer to EDS for GPIO pads IRQ numbers (PADCFG\_DW1.IntSel) If GPIO is under GPIO OS driver control and appropriate ACPI GpioInt descriptor exist then use only trigger type setting (from GpioIntLevel to GpioIntBothEdge). This type of GPIO Driver interrupt doesn't have any additional routing setting required to be set by BIOS. Interrupt is handled by GPIO OS Driver.

## Enumerator

- GpioIntDefault** Leave value of interrupt routing unmodified.
- GpioIntDis** Disable IOxAPIC/SCI/SMI/NMI interrupt generation.
- GpioIntNmi** Enable NMI interrupt only.
- GpioIntSmi** Enable SMI interrupt only.
- GpioIntSci** Enable SCI interrupt only.
- GpioIntApic** Enable IOxAPIC interrupt only.
- GpioIntLevel** Set interrupt as level triggered.
- GpioIntEdge** Set interrupt as edge triggered (type of edge depends on input inversion)
- GpioIntLvlEdgDis** Disable interrupt trigger.
- GpioIntBothEdge** Set interrupt as both edge triggered.

Definition at line 207 of file GpioConfig.h.

## 9.7.2.6 enum GPIO\_LOCK\_CONFIG

GPIO LockConfiguration Set GPIO configuration lock and output state lock.

GpioLockPadConfig and GpioLockOutputState can be OR'ed. Lock settings reset is in Powergood domain. Care must be taken when using this setting as fields it locks may be reset by a different signal and can be controllable by what is in GPIO\_RESET\_CONFIG (PADCFG\_DW0.PadRstCfg). GPIO library provides functions which allow to unlock a GPIO pad.

## Enumerator

- GpioLockDefault** Leave lock setting unmodified.
- GpioPadConfigLock** Lock Pad Configuration.
- GpioOutputStateLock** Lock GPIO pad output value.

Definition at line 329 of file GpioConfig.h.

## 9.7.2.7 enum GPIO\_OTHER\_CONFIG

Other GPIO Configuration GPIO\_OTHER\_CONFIG is used for less often settings and for future extensions Supported settings:

- RX raw override to '1' - allows to override input value to '1' This setting is applicable only if in input mode (both in GPIO and native usage). The override takes place at the internal pad state directly from buffer and before the RXINV.

## Enumerator

- GpioRxRaw1Default** Use default input override value.
- GpioRxRaw1Dis** Don't override input.
- GpioRxRaw1En** Override input to '1'.

Definition at line 346 of file GpioConfig.h.

## 9.7.2.8 enum GPIO\_OUTPUT\_STATE

GPIO Output State This field is relevant only if output is enabled.



## Enumerator

**GpioOutDefault** Leave output value unmodified.

**GpioOutLow** Set output to low.

**GpioOutHigh** Set output to high.

Definition at line 181 of file GpioConfig.h.

## 9.7.2.9 enum GPIO\_PAD\_MODE

GPIO Pad Mode Refer to GPIO documentation on native functions available for certain pad.

If GPIO is set to one of NativeX modes then following settings are not applicable and can be skipped:

- Interrupt related settings
- Host Software Ownership
- Output/Input enabling/disabling
- Output lock

Definition at line 132 of file GpioConfig.h.

## 9.7.2.10 enum GPIO\_RESET\_CONFIG

GPIO Power Configuration GPIO\_RESET\_CONFIG allows to set GPIO Reset type (PADCFG\_DW0.PadRstCfg) which will be used to reset certain GPIO settings.

Refer to EDS for settings that are controllable by PadRstCfg.

## Enumerator

**GpioResetDefault** Leave value of pad reset unmodified.

**GpioResetPwrGood** Deprecated settings. Maintained only for compatibility. GPP: RSMRST; GPD: DSW\_↔ PWROK; (PadRstCfg = 00b = "Powergood")

**GpioResetDeep** Deep GPIO Reset (PadRstCfg = 01b = "Deep GPIO Reset")

**GpioResetNormal** GPIO Reset (PadRstCfg = 10b = "GPIO Reset" )

**GpioResetResume** GPP: Reserved; GPD: RSMRST; (PadRstCfg = 11b = "Resume Reset" )

**GpioResumeReset** New GPIO reset configuration options. Resume Reset (RSMRST) GPP: PadRstCfg = 00b = "Powergood" GPD: PadRstCfg = 11b = "Resume Reset" Pad setting will reset on:

- DeepSx transition
- G3 Pad settings will not reset on:
- S3/S4/S5 transition
- Warm/Cold/Global reset

**GpioHostDeepReset** Host Deep Reset PadRstCfg = 01b = "Deep GPIO Reset" Pad settings will reset on:

- Warm/Cold/Global reset
- DeepSx transition
- G3 Pad settings will not reset on:
- S3/S4/S5 transition

**GpioPlatformReset** Platform Reset (PLTRST) PadRstCfg = 10b = "GPIO Reset" Pad settings will reset on:

- S3/S4/S5 transition
- Warm/Cold/Global reset
- DeepSx transition

- G3

**GpioDswReset** Deep Sleep Well Reset (DSW\_PWROK) GPP: not applicable GPD: PadRstCfg = 00b = "↔ Powergood" Pad settings will reset on:

- G3 Pad settings will not reset on:
- S3/S4/S5 transition
- Warm/Cold/Global reset
- DeepSx transition

Definition at line 229 of file GpioConfig.h.

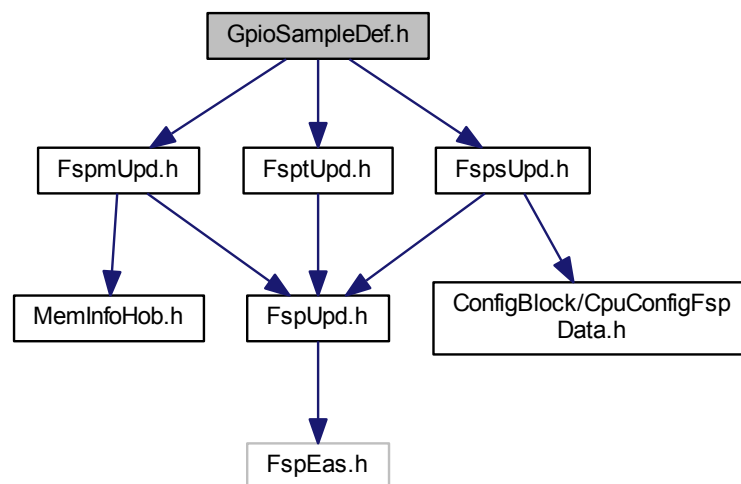
## 9.8 GpioSampleDef.h File Reference

```
#include <FsptUpd.h>
```

```
#include <FspmUpd.h>
```

```
#include <FspsUpd.h>
```

Include dependency graph for GpioSampleDef.h:



### 9.8.1 Detailed Description

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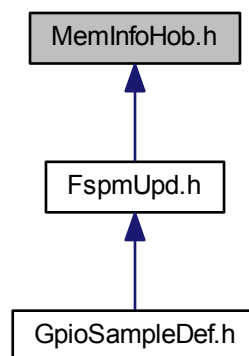
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## 9.9 MemInfoHob.h File Reference

This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs.

This graph shows which files directly or indirectly include this file:



### Classes

- struct [DIMM\\_INFO](#)  
*Memory SMBIOS & OC Memory Data Hob.*
- struct [MEMORY\\_PLATFORM\\_DATA](#)  
*Memory Platform Data Hob.*

### Macros

- #define [WARM\\_BOOT](#) 2  
*Host reset states from MRC.*
- #define [MAX\\_SPD\\_SAVE](#) 29  
*Defines taken from MRC so avoid having to include MrcInterface.h.*

### 9.9.1 Detailed Description

This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs.

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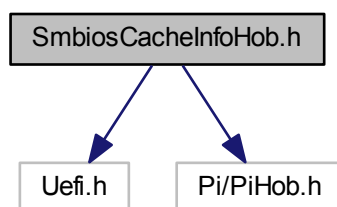
#### Specification Reference:

## 9.10 SmbiosCacheInfoHob.h File Reference

Header file for SMBIOS Cache Info HOB.

```
#include <Uefi.h>
#include <Pi/PiHob.h>
```

Include dependency graph for SmbiosCacheInfoHob.h:



#### Classes

- struct [SMBIOS\\_CACHE\\_INFO](#)  
*SMBIOS Cache Info HOB Structure.*

### 9.10.1 Detailed Description

Header file for SMBIOS Cache Info HOB.

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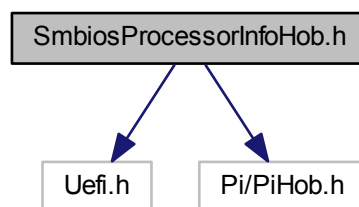
#### Specification Reference:

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## 9.11 SmbiosProcessorInfoHob.h File Reference

Header file for SMBIOS Processor Info HOB.

```
#include <Uefi.h>
#include <Pi/PiHob.h>
Include dependency graph for SmbiosProcessorInfoHob.h:
```



#### Classes

- struct [SMBIOS\\_PROCESSOR\\_INFO](#)  
*SMBIOS Processor Info HOB Structure.*

### 9.11.1 Detailed Description

Header file for SMBIOS Processor Info HOB.

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**Specification Reference:**

System Management BIOS (SMBIOS) Reference Specification v3.0.0 dated 2015-Feb-12 (DSP0134) [http://www.dmtf.org/sites/default/files/standards/documents/DSP0134\\_3.0.0.pdf](http://www.dmtf.org/sites/default/files/standards/documents/DSP0134_3.0.0.pdf)

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