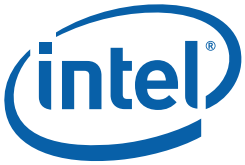


Menlow Platform Crown Beach Customer Enabling Board

Schematics

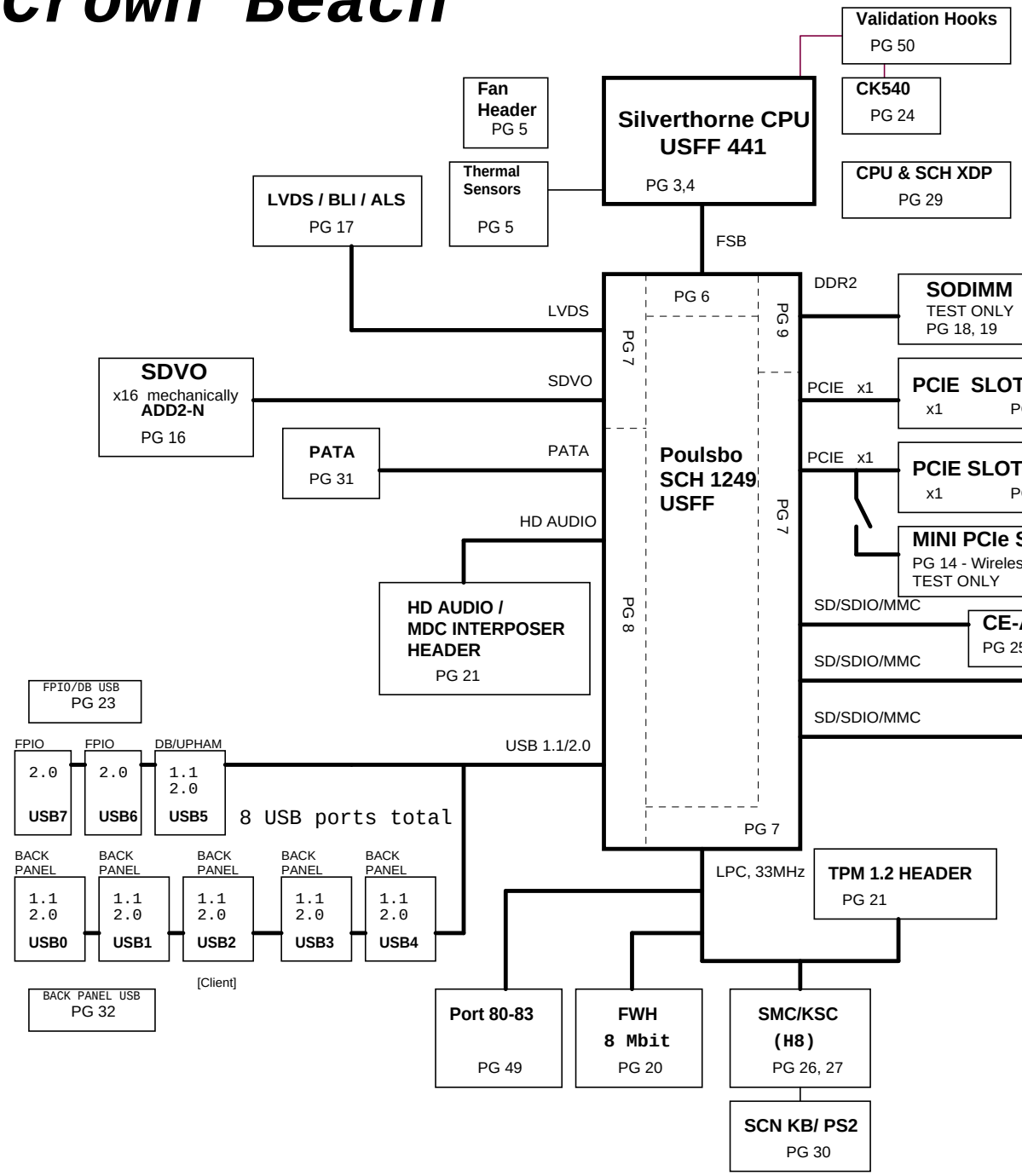
November 2007

Revision 1.5

Intel Confidential

Crown Beach

Menlow Platform Validation Vehicle and Customer Enabling Board (Silverthorne / Poulsbo) Rev 1.5 (ES2)



Voltage Rails

POWER PLANE	ON STATE
+V1.05S_SCH	S0
+V1.05S_VTT	S0
+V1.05_SUS	S0, S3 (IF NEEDED)
+V1.5S	S0
+V1.5_SUS	S0, S3 (IF NEEDED)
+V1.8	S0, S3
+V3.3	S0, S3
+V3.3S	S0
+V3.3A	S0, S3, S4/S5
+V3.3_SCH	S0, S3
+V3.3S_SCH	S0
+V3.3_SLOTS	S0
+V5	S0, S3
+V5S	S0
+V5A	S0, S3, S4/S5
+V12	S0, S3
+V12S	S0
+V12_ATX	S0, S3, S4/S5
+V12_SLOTS	S0

IMVP-6 VR PG 41,42,43

DDR2 VR PG 36

POULSBO 1.5V VR PG 38

+V1.05SUS & +V1.5SUS & DDR2 VREF PG 37

POULSBO CORE 1.05V & FSBVTT 1.05V VR PG 33

SYSTEM (3.3V & 5V) VR PG 39

EV Margining PG 48

ATX POWER CONN PG 44

POWER SEQUENCING PG 47

ENABLES & PWRGDs PG 40

Crown Beach		Intel Confidential
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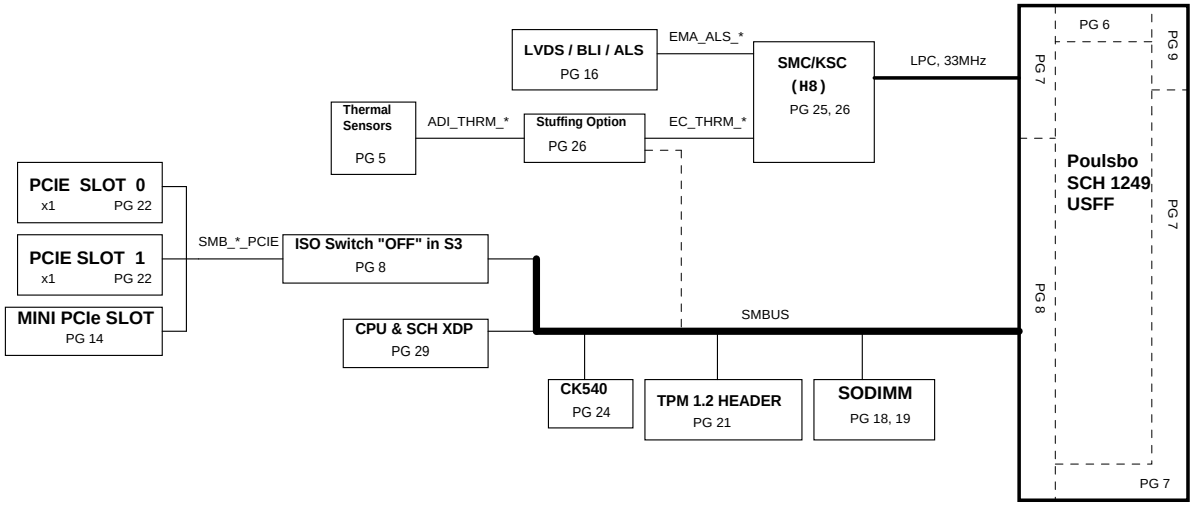
CROWN BEACH VALIDATION VEHICLE

SMBUS DIAGRAM, JUMPER SETTINGS, LED / SWITCHES, AND MISC BOARD INFORMATION



I²C / SMB Addresses

Page	Device	Hex Address	Bus
5	CPU Thermal Sensor	2E	EC_THRM_CLK, EC_THRM_DATA
5	DDR Thermal Sensor	4C	EC_THRM_CLK, EC_THRM_DATA
18	SO-DIMM0	A0	SMB_CLK, SMB_DATA
21	TPM MODULE	N/A	SMB_CLK, SMB_DATA
24	Clock Generator - CK540	D2/D3	SMB_CLK, SMB_DATA
29	XDP	N/A	SMB_CLK, SMB_DATA

LEDs and Switches

LED	Page
Mini WWAN	14
Mini WLAN	14
Mini WPAN	14
SDIO Slot 0	25
SDIO Slot 1	25
SDIO Slot 2	25
SMC/KBC Caps lock	26
SMC/KBC Scroll lock	26
SMC/KBC Num lock	26
PATA Active	31
VID 0	34
VID 1	34
VID 2	34
VID 3	34
VID 4	34
VID 5	34
VID 6	34
H_IERR#	35
CPU_MCERR#	35
SMC On/Off	46
Reset	46
PM_RSMRST	46
S0 State	46
S3 State	46
S4/S5 State	46
Always Powergood	46
PM_DELAY_VR_PWRGD	46
SCH_PWROK	46
PM_RSMRST_PWRGD	46
High nibble Port 80/82	49
Low nibble Port 80/82	49
High nibble Port 81/83	49
Low nibble Port 81/83	49

Switch	Page
Lid	27
Virtual battery	27
Power On/Off	44
Reset	44

Header Shunt Settings

Default	Description	Page
1-2	H_THERMDA	5
3-4	H_THERMDC	5
1-X	CMOS EN	4
1-X	RTC Reset	7
N/A	MFG/TEST	8
1-2	CPV MFG/TEST	8
2-3	SCH CFG0	12
2-3	SCH CFG1	12
1-2	Slot2 D2 Mini	14
1-2	WiFi Host Wake	14
1-2	V3.3 Mini PCIe	14
1-2	PMU_1	14
1-2	PMU_2	14
1-2	GPS UART CTS	14
1-2	GPS On	14
1-2	EC_WiFi PD#	14
1-2	PMU_3	14
1-2	PMU_4	14
2-3	Mini PCIe Power	15
1-2	PMU_1	15
1-2	PMU_2	15
1-2	PMU_3	15
1-2	PMU_4	15
1-X	RECOVERY	20
1-2	VCCHDA SEL	21
2-3	BSEL2	24
1-X	BSEL1	24
1-X	CE_ATA Select(TEST)	25
1-X	SDIO Slot1 CD	25
1-X	SDIO Slot2 CD	25
1-2	EC_RST#	26
1-2	MDO	26
1-2	MD1	26
1-X	KBC DISABLE (NO-OP)	26
1-X	Normal Oper	26
1-X	H8 JTAG	26
1-X	LID JMPR	27
1-X	V8 JMPR	27
1-2	PM_SLP_S3#	27
1-X	XDP TCK 0 to 1	29
1-2	XDP TDI	29
1-2	XDP TDO to TDI	29
1-2	XDP TDE Reset	29
1-2	BOOT BLOCK PROG	30
1-2	PATA PRELOAD	31
1-X	Enable 5V Load	40
1-2	Disable 12V Load	40
1-2	IMVP-6 STRAP_VID6	41
3-4	IMVP-6 STRAP_VID5	41
5-6	IMVP-6 STRAP_VID4	41
7-8	IMVP-6 STRAP_VID3	41
9-10	IMVP-6 STRAP_VID2	41
11-12	IMVP-6 STRAP_VID1	41
13-14	IMVP-6 STRAP_VID0	41
1-2	SLPIOVR#C6	43
1-X	PORT 80-81	49
1-2	Manara VIDs	50
	ADDITIONAL HOOKS FOR TEST ONLY	
1-2	Port1 RS232 Mode	56
1-2	Port2 RS232 Mode	56
1-2	Port1 RS232 Mode	56
1-2	Port2 RS232 Mode	56

Default Jumper Settings For Stuffed Jumpers

1-X means jumper is parked on one pin.

H8 KBC & SMC all refer to different functions & names of embedded controller.

Wake Events

Wake Events	State Supported
PCI Express wake event	S3
LID switch attached to SMC	S3
USB	S3
Hot Key from Scan matrix keyboard	S3
PS/2 Keyboard/mouse	S3
PWRBTN#	S3, S4, S5

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Title: Notes		
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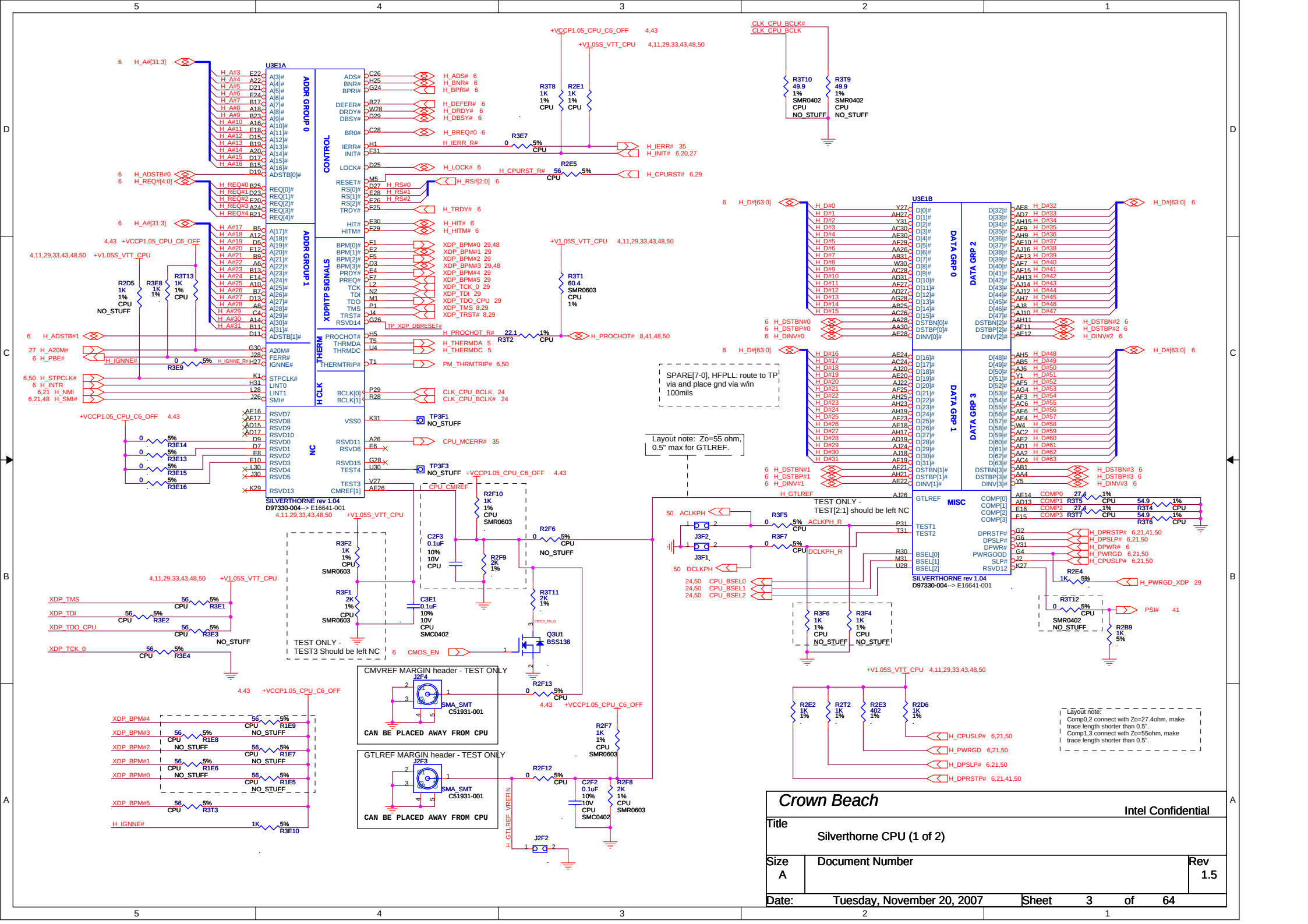
U3E1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
NC
SILVERTHORNE rev 1.04
D97330-004--> E16641-001
U3E1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SILVERTHORNE rev 1.04
D97330-004--> E16641-001
SPARE[7-0], HFPLL: route to TP via and place gnd via w/in 100mils
Layout note: Zo=55 ohm, 0.5" max for GTLREF.
TEST ONLY - TEST[2:1] should be left NC
TEST ONLY - TEST3 Should be left NC
CMVREF MARGIN header - TEST ONLY
GTLREF MARGIN header - TEST ONLY
CAN BE PLACED AWAY FROM CPU
CAN BE PLACED AWAY FROM CPU
Layout note:
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".
Crown Beach
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Title
Silverthorne CPU (1 of 2)
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Rev
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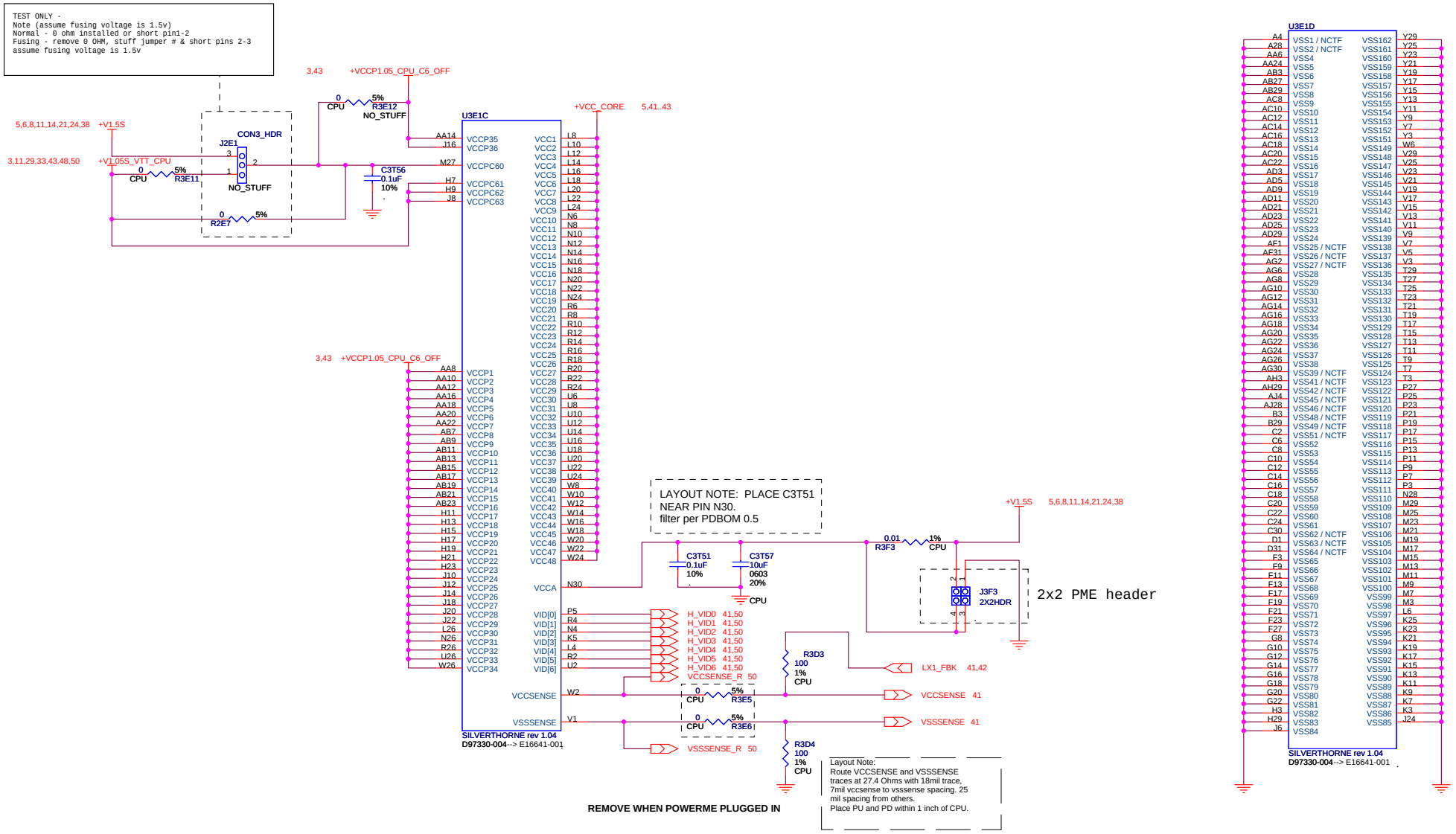

Crown Beach		Intel Confidential
Title: Silverthorne CPU (2 of 2)		
Size: A	Document Number	Rev: 1.5
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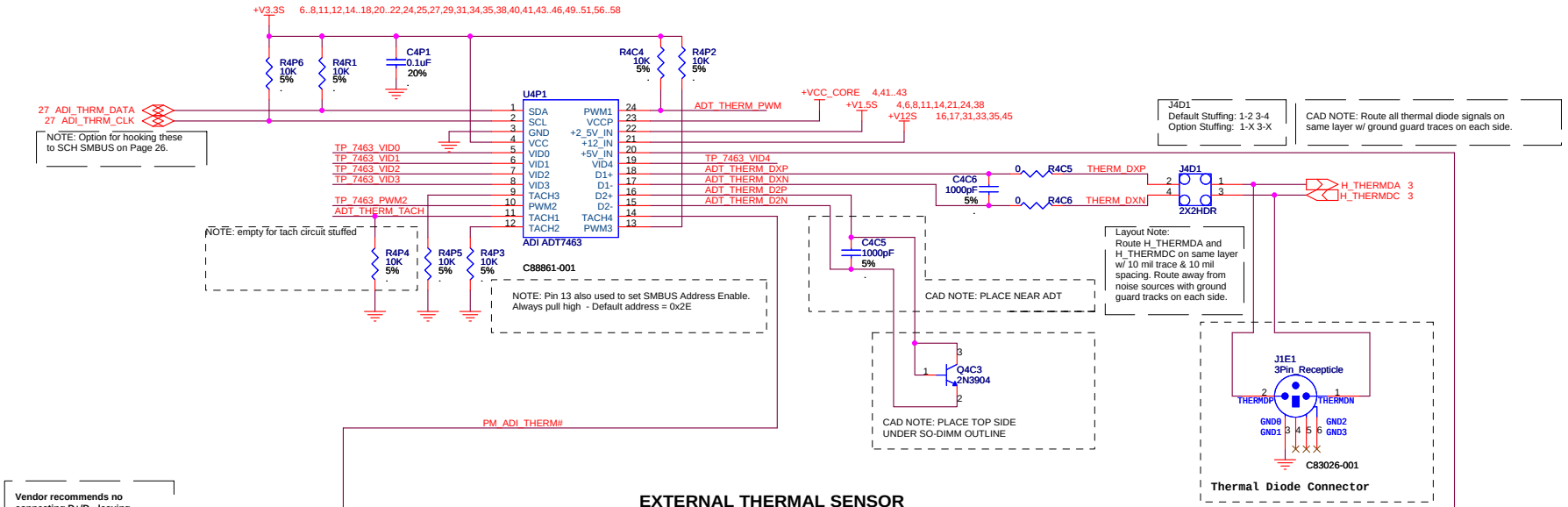
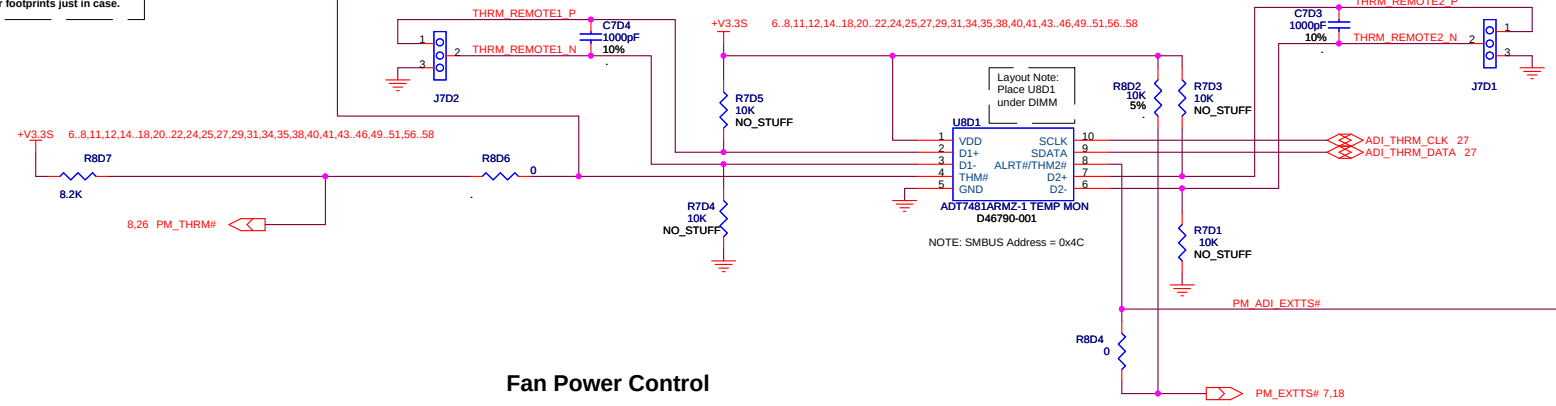
CPU Thermal Sensors

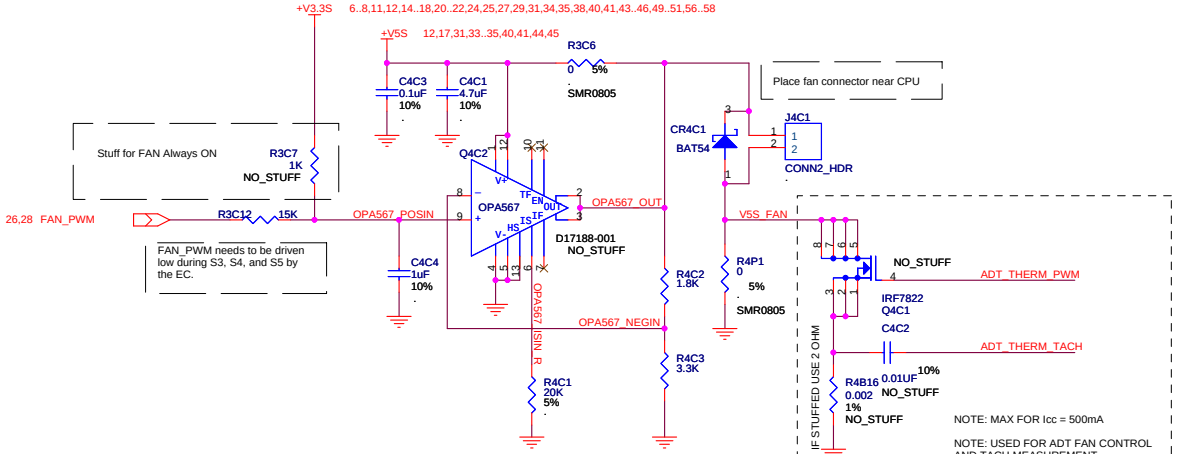


Vendor recommends no connecting D+/D-, leaving resistor footprints just in case.

EXTERNAL THERMAL SENSOR



Fan Power Control



Crown Beach		Intel Confidential
Title: CPU Thermal Sensor & Fan		
Size: A	Document Number	Rev: 1.5
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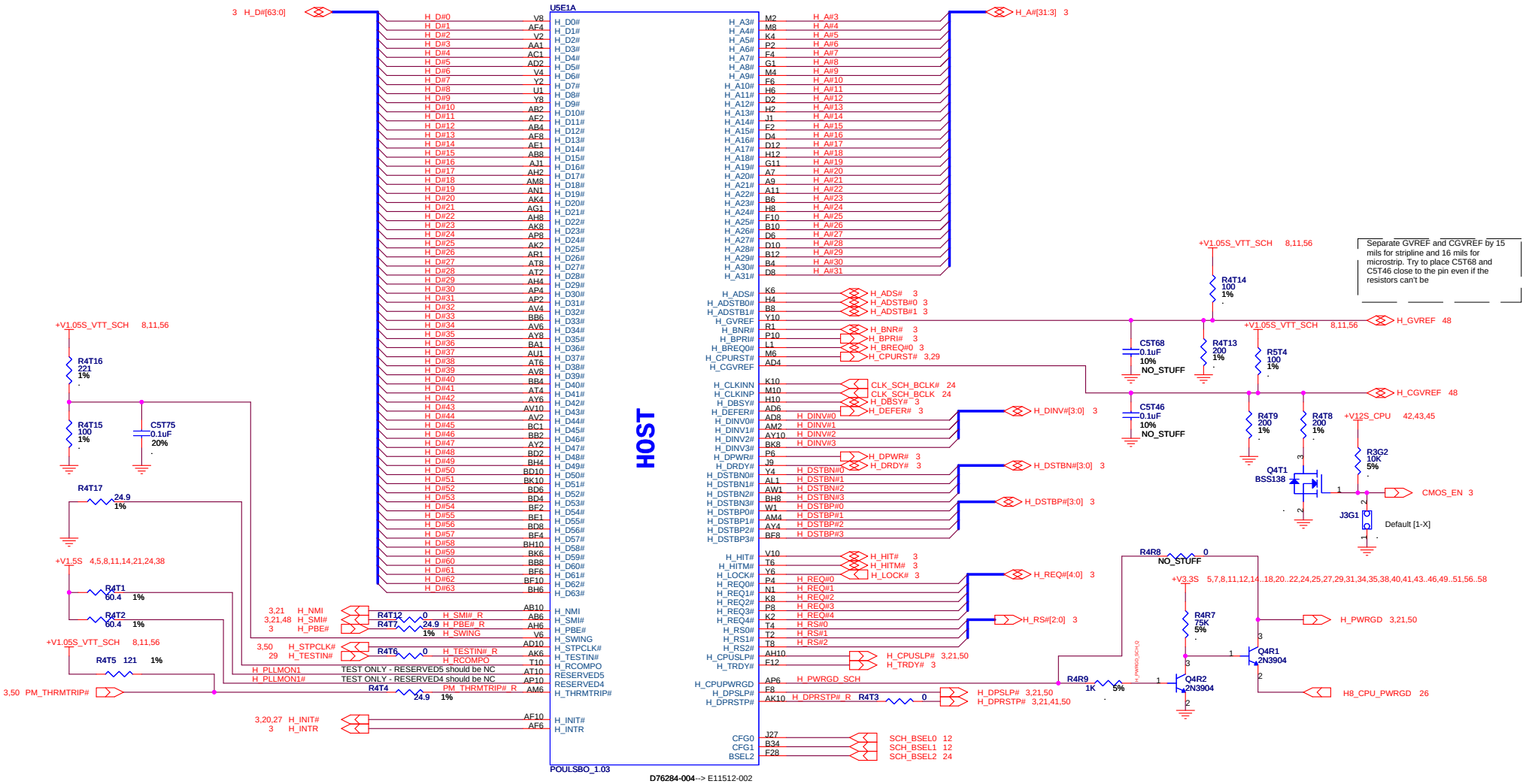

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Title: Poulsbo (1 of 8)			
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CAD NOTE: Place all series resistors near the SCH and place all 10 pF caps near farthest component clocked by the LPC bus (For EV testing)

SCH internal VR enable strap for +V1.5 & +V1.05 VRs

	INTVRMEN	R4H2	R4H1
Enable (default)	1	STUFF	UNSTUFF
Disable		UNSTUFF	STUFF

RTC Circuitry

RTC_Reset	J4H1
Clear RTC	Shunt
Keep RTC	Open 1-X (Default)

SLPRDY#	SLPMODE	
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5

Test Only -
Poulsbo SCH pin G21 should be left NC on production designs

Route PEG_COMP less than 250 milliohm trace impedance.

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Title: Poulsbo (2 of 8)			
Size: A	Document Number		Rev: 1.5
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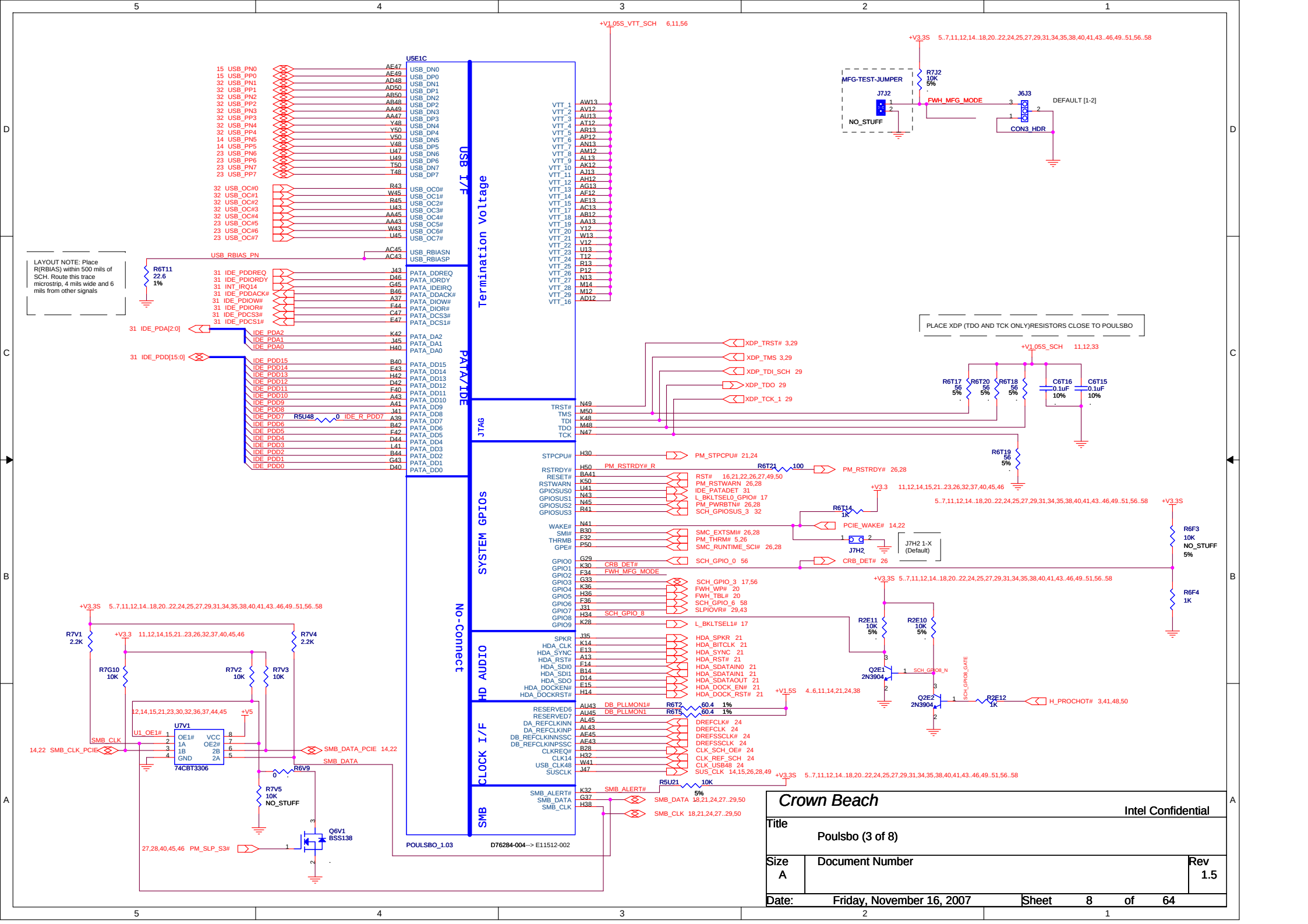
U5E1C
USB I/F
Termination Voltage
PATA/IDE
JTAG
SYSTEM GPIOs
HD AUDIO
CLOCK I/F
SMB
No-Connect
LAYOUT NOTE: Place R(RBIAS) within 500 mils of SCH. Route this trace microstrip, 4 mils wide and 6 mils from other signals
PLACE XDP (TDO AND TCK ONLY)RESISTORS CLOSE TO POULSBO
MFG-TEST-JUMPER
NO_STUFF
DEFAULT [1-2]
CON3_HDR
J7H2 1-X (Default)
74CBT3306
Q2E1 2N3904
Q2E2 2N3904
Q6V1 BSS138
POULSBO_1.03
D76284-004--> E11512-002
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Poulsbo (3 of 8)
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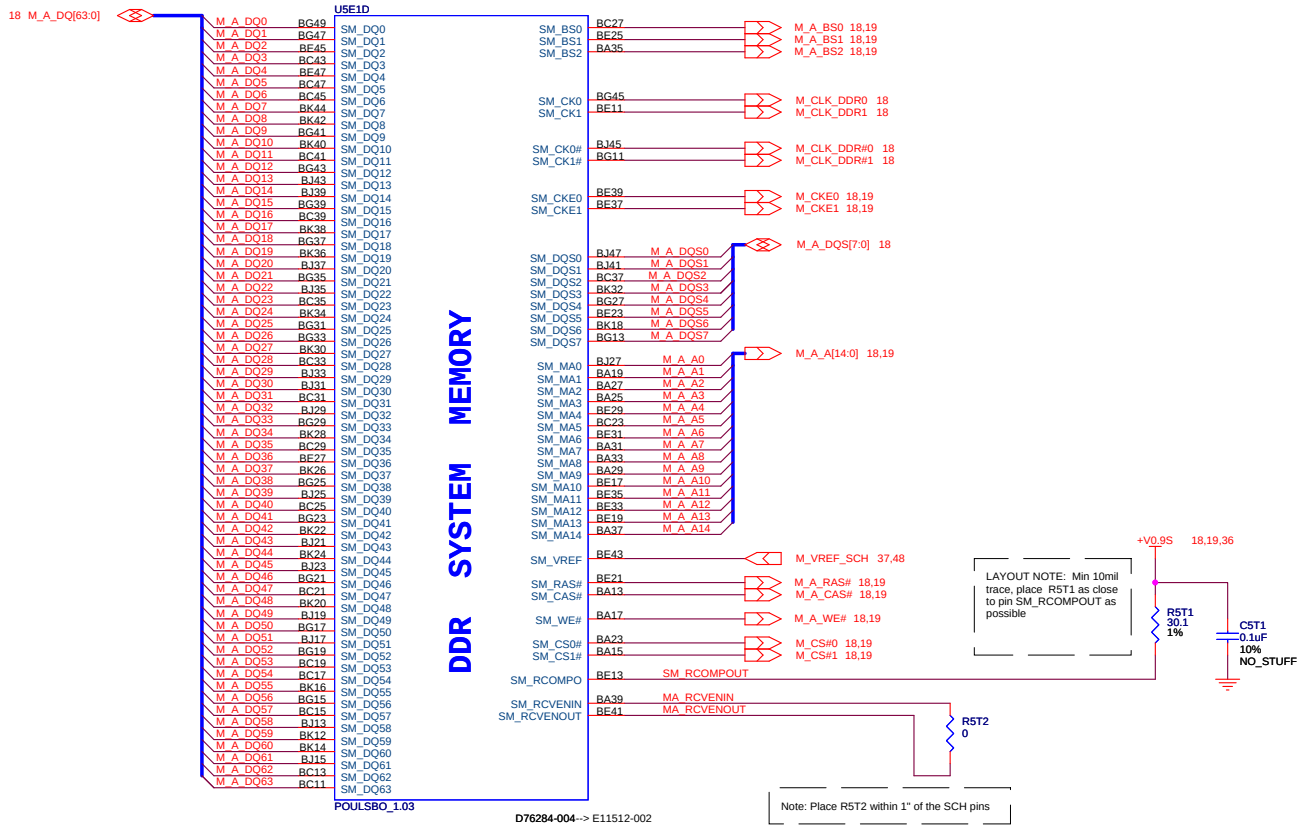

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Title: Poulsbo (4 of 8)		
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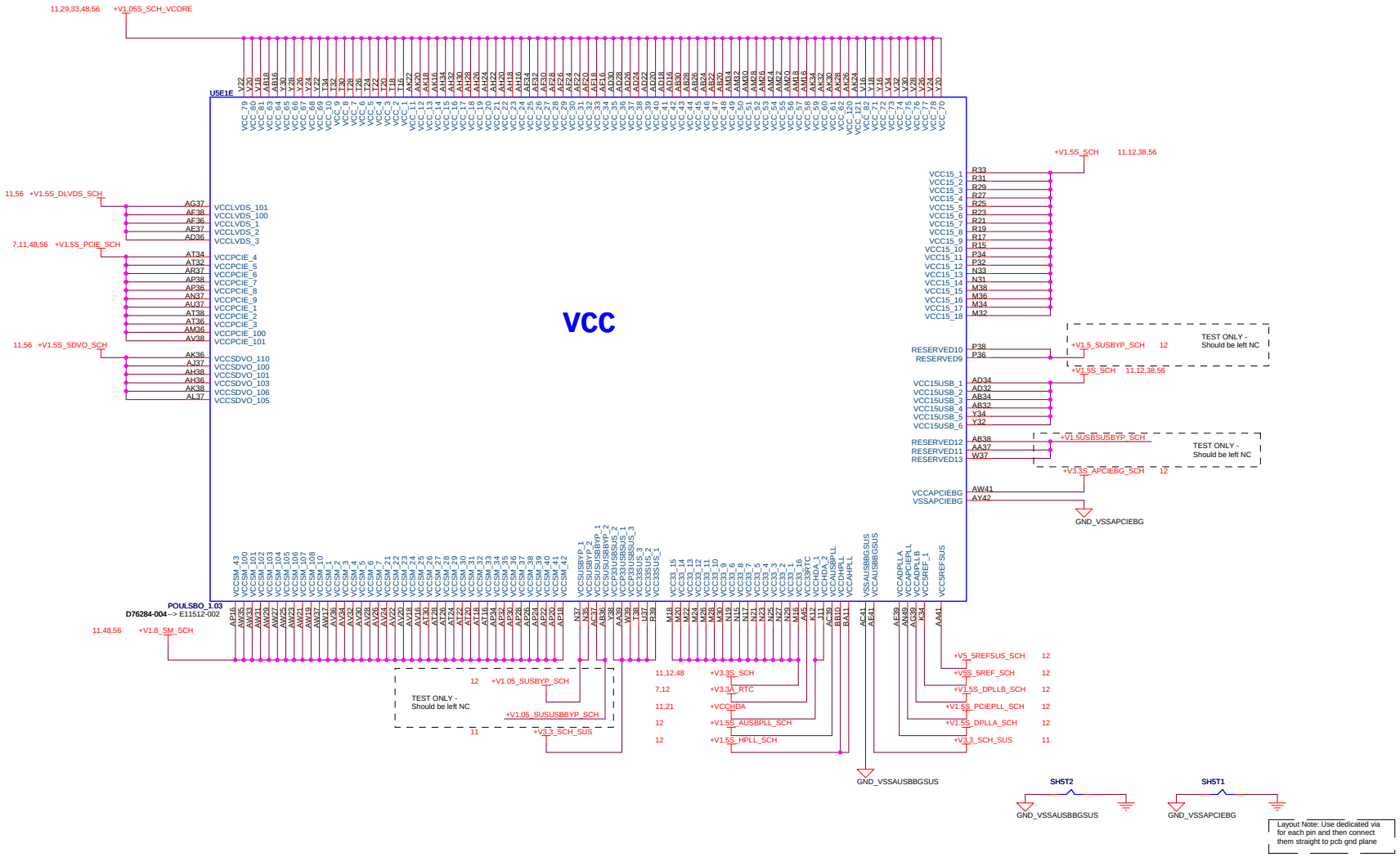

Crown Beach			Intel Confidential
Title	Poulsbo (5 of 8) VCC-PWR		
Size: Custom	Document Number		Rev: 1.5
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All decoupling should be placed on the backside

8,12,33 +V1.05S_SCH — R6T7 0.01_1% SMR1206 — 10,29,33,48,56 +V1.05S_SCH_VCORE

C6T7 4.7uF 10% SMC0603; C6T8 270uF 20% SMC7343

C5T41 0.1uF 10% SMC0402; C5T31 0.1uF 10% SMC0402; C5T32 0.1uF 10% SMC0402; C5T67 1.0uF 20% NO_STUFF SMC0402; C5T52 1.0uF 20% NO_STUFF SMC0402; C5T64 1.0uF 20% NO_STUFF SMC0402; C5T40 1.0uF 20% NO_STUFF SMC0402; C5T74 1.0uF 20% NO_STUFF SMC0402; C5T29 1.0uF 20% NO_STUFF SMC0402; C5T42 1.0uF 20% NO_STUFF SMC0402; C5T30 1.0uF 20% NO_STUFF SMC0402; C5T27 1.0uF 20% NO_STUFF SMC0402; C5T39 1.0uF 20% NO_STUFF SMC0402; C5T53 1.0uF 20% NO_STUFF SMC0402; C5T51 2.2uF SMC0402; C5T66 2.2uF SMC0402; C6T9 10uF 20% NO_STUFF 0603; C6T10 10uF 20% NO_STUFF 0603; C5T33 10uF 20% NO_STUFF 0603; C5T34 10uF 20% NO_STUFF 0603; C6T14 10uF 20% SMC0805; C6T13 10uF 20% SMC0805; C6T11 10uF 20% SMC0805; C6T12 10uF 20% SMC0805; C5T38 PH0201 10% NO_STUFF; C5T65 PH0201 10% NO_STUFF

24,33,34 +V1.05S_VTT — R5U35 0.01_1% SMR1206 — 6,8,56 +V1.05S_VTT_SCH

C5U8 4.7uF 10% SMC0603; C5U11 270uF 20% SMC7343

C5T36 1.0uF 20% NO_STUFF SMC0402; C5T71 1.0uF 20% SMC0402; C5T56 1.0uF 20% NO_STUFF SMC0402; C5T28 1.0uF 20% NO_STUFF SMC0402; C5T47 1.0uF 20% SMC0402; C5T26 1.0uF 20% SMC0402; C5T63 1.0uF 20% NO_STUFF SMC0402; C5T62 1.0uF 20% NO_STUFF SMC0402; C5T50 1.0uF 20% NO_STUFF SMC0402; C5T43 1.0uF 20% NO_STUFF SMC0402; C5T37 1.0uF 20% NO_STUFF SMC0402; C5T70 1.0uF 20% NO_STUFF SMC0402; C5T78 1.0uF 20% NO_STUFF SMC0402; C5T35 1.0uF 20% NO_STUFF SMC0402; C5T24 1.0uF 20% NO_STUFF SMC0402; C5T54 1.0uF 20% NO_STUFF SMC0402; C5U7 10uF 20% NO_STUFF SMC0805; C5U2 10uF 20% SMC0805; C5U4 10uF 20% NO_STUFF SMC0805; C5U6 10uF 20% SMC0805

4..6,8,14,21,24,38 +V1.5S — R5T6 — 10,12,38,56 +V1.5S_SCH

C5U1 4.7uF 10% SMC0603

C5T80 1.0uF 20% SMC0402; C5T72 1.0uF 20% SMC0402; C5T81 1.0uF 20% SMC0402; C5T57 1.0uF 20% SMC0402; C5T86 1.0uF 20% SMC0402; C5T79 1.0uF 20% SMC0402; C5T85 1.0uF 20% SMC0402

24,33,34 +V1.05S_VTT — +V1.05S_VTT_CPU 3,4,29,33,43,48,50

R3U1 .01 1% SMR2010

C3T17 0.1uF 10% SMC0402; C3T19 0.1uF 10% SMC0402; C2T1 0.1uF 10%; C3T16 0.1uF 10%; C2T3 0.1uF 10%; C3T1 0.1uF 10%

Place these inside socket cavity on L8 (North side Secondary)

J4F5 2X2HDR

2x2 PME header

10,12,38,56 +V1.5S_SCH — R6T6 — +V1.5S_PCIE_SCH 7,10,48,56

C5T25 1.0uF 20% SMC0402; C5T19 1.0uF 20% SMC0402

LAYOUT NOTE: PLACE CAPS NEXT TO CPU PINS AG35 AND AG36

10,12,38,56 +V1.5S_SCH — R6T9 — +V1.5S_DLVDS_SCH 10,56

C5T55 1.0uF 20% SMC0402; C5T48 1.0uF 20% SMC0402

10,12,38,56 +V1.5S_SCH — R6T10 — +V1.5S_SDVO_SCH 10,56

C5T44 1.0uF 20% SMC0402; C5T45 1.0uF 20% SMC0402

8,12,14,15,21..23,26,32,37,40,45,46 +V3.3 — +V3.3_SCH_SUS 10

R6T13 0.01 1% SMR0805

C5T59 0.1uF 10% SMC0402; C5T60 0.1uF 10% SMC0402; C5T61 0.1uF 10% SMC0402; C5T58 0.1uF 10% SMC0402; C5T69 0.1uF 10% NO_STUFF SMC0402

GND_VSSAUSBBGSUS

18,36,37 +V1.8 — R5T3 — +V1.8_SM_SCH 10,48,56

C6T3 4.7uF 10% SMC0603

C5T12 1.0uF 20% NO_STUFF SMC0402; C5T23 1.0uF 20% NO_STUFF SMC0402; C5T5 1.0uF 20% NO_STUFF SMC0402; C5T21 1.0uF 20% SMC0402; C5T20 1.0uF 20% SMC0402; C5T15 1.0uF 20% NO_STUFF SMC0402; C5T11 1.0uF 20% NO_STUFF SMC0402; C5T9 1.0uF 20% NO_STUFF SMC0402; C5T10 1.0uF 20% NO_STUFF SMC0402; C5T22 1.0uF 20% NO_STUFF SMC0402; C5T7 1.0uF 20% SMC0402; C5T18 1.0uF 20% NO_STUFF SMC0402; C5T13 1.0uF 20% NO_STUFF SMC0402; C5T6 1.0uF 20% NO_STUFF SMC0402; C5T17 1.0uF 20% NO_STUFF SMC0402; C5T16 1.0uF 20% NO_STUFF SMC0402; C5T8 1.0uF 20% NO_STUFF SMC0402

+V3.3S 5..8,12,14..18,20..22,24,25,27,29,31,34,35,38,40,41,43..46,49..51,56..58 — R5T5 — +V3.3S_SCH 10,12,48

C5T92 4.7uF 10% SMC0603

C5T84 1.0uF 20% SMC0402; C5T87 1.0uF 20% SMC0402; C5T88 1.0uF 20% SMC0402; C5T90 1.0uF 20% SMC0402

+VCCHDA 10,21

C5U3 1.0uF 20% SMC0402; C5T91 1.0uF 20% SMC0402

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Title: Poulsbo (6 of 8) SCH Decoupling		
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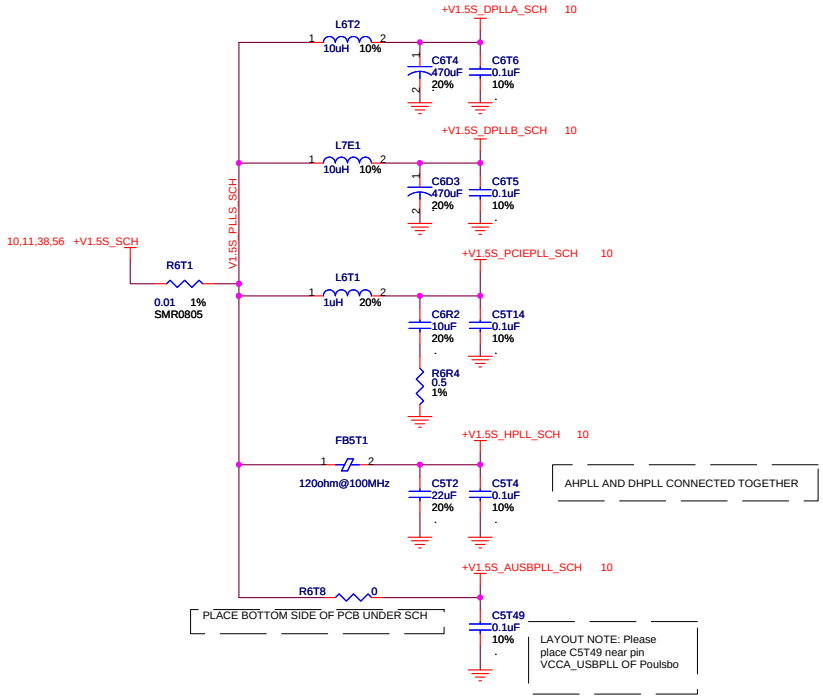
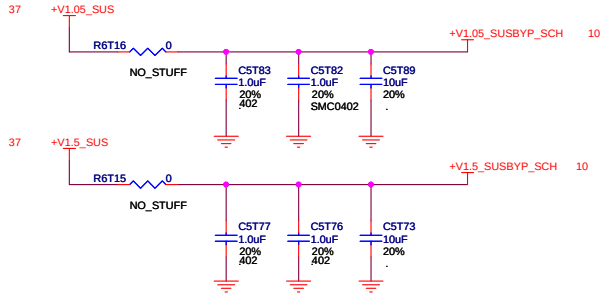
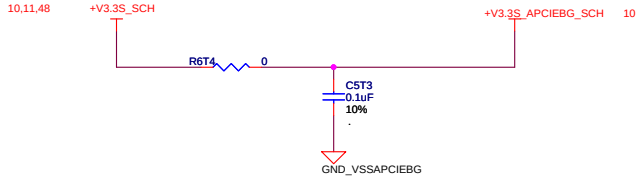
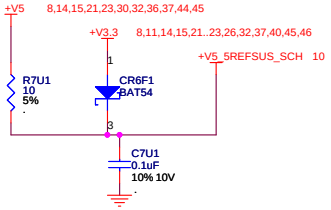
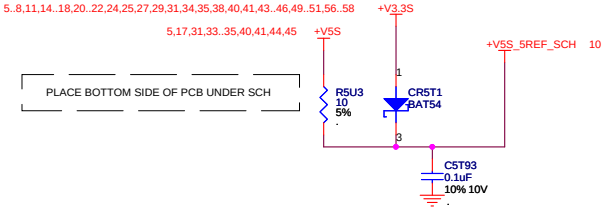
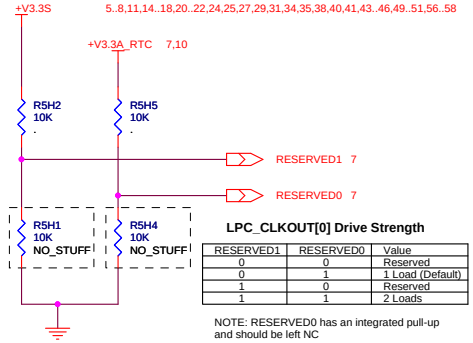








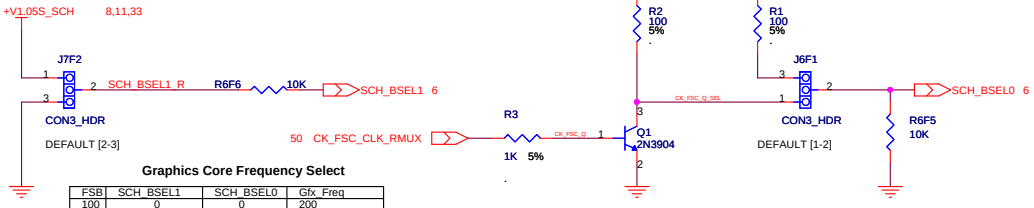




LPC_CLKOUT[0] Drive Strength

RESERVED1	RESERVED0	Value
0	0	Reserved
0	1	1 Load (Default)
1	0	Reserved
1	1	2 Loads

NOTE: RESERVED0 has an integrated pull-up and should be left NC



Graphics Core Frequency Select

FSB	SCH_BSEL1	SCH_BSEL0	Gfx_Freq
100	0	0	200
100	0	1	RESERVED
100	1	0	RESERVED
100	1	1	RESERVED
133	0	0	RESERVED
133	0	1	200
133	1	0	RESERVED
133	1	1	RESERVED

Note: Clock Frequencies are in Mhz
Default Frequency determined by FSB speed
Position 1-2 = 1 Position 2-3 = 0

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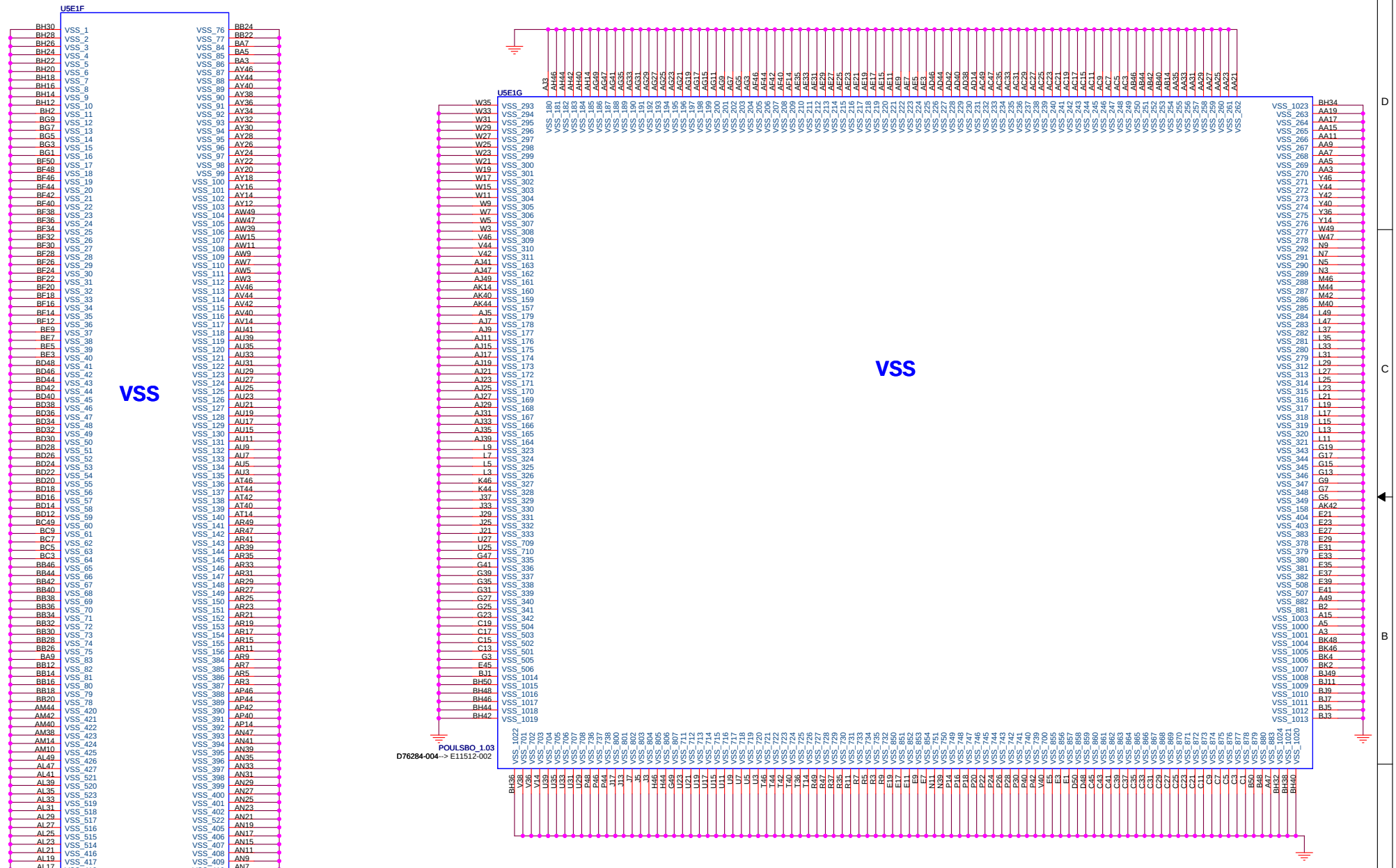
Title: Poulsbo (7 of 8) SCH-Pu/Pd

Size	Document Number	Rev
A		1.5

Date: Tuesday, November 20, 2007 Sheet 12 of 64



Crown Beach		Intel Confidential
Title	Poulsbo (8 of 8) VSS-GND	
Size A	Document Number	Rev 1.5
Date: Friday, November 16, 2007	Sheet 13 of 64	

CONNECTOR A

WIFI_nINTR requested by Gopi

PLACE NEAR SCH

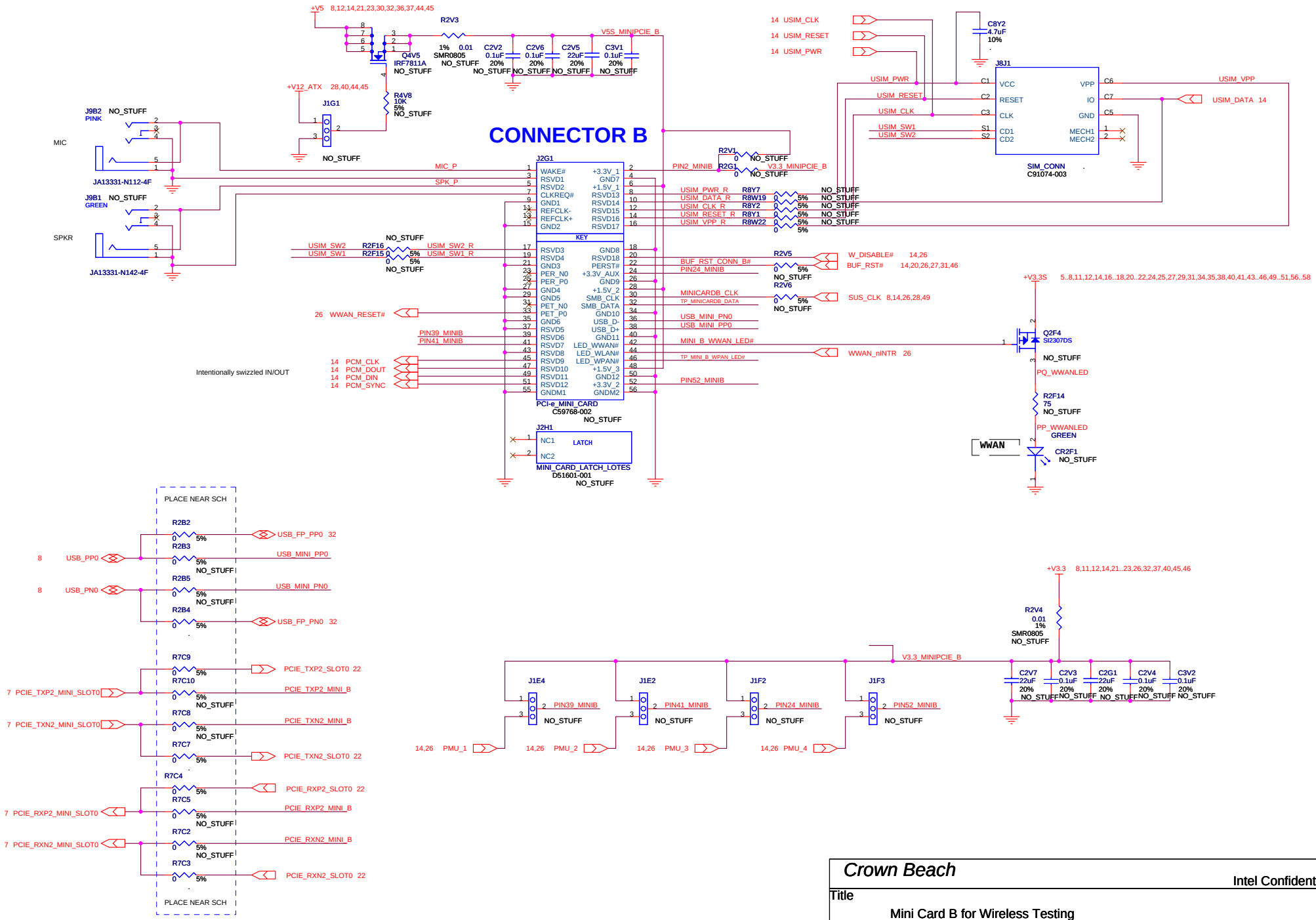
PLACE NEAR SCH

COM Port option

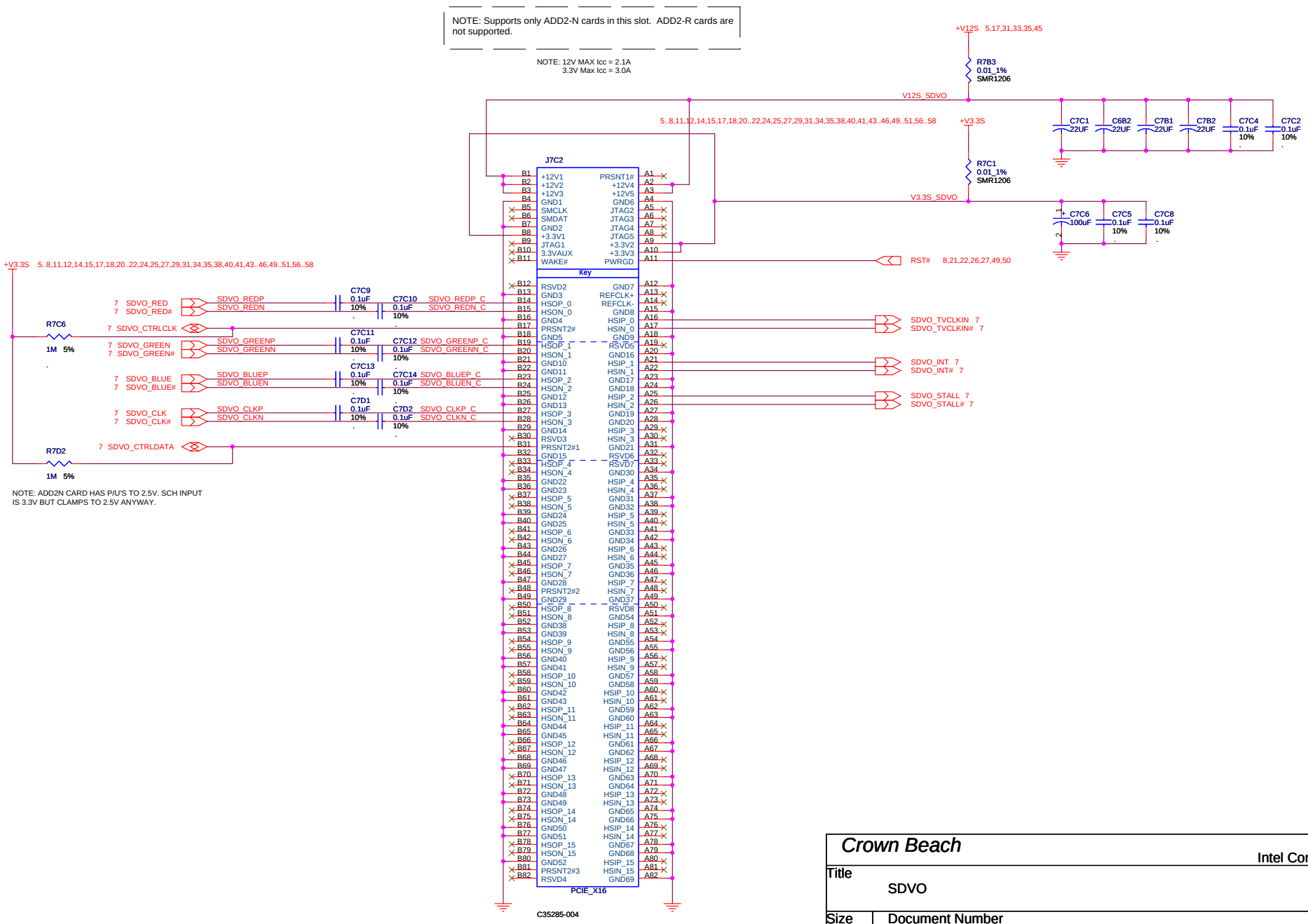
RS232 bypass option
Place near U6E4

Crown Beach		Intel Confidential
Title: Mini Card A For Wireless Testing		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 14 of 64	

CONNECTOR B



Crown Beach		Intel Confidential
Title: Mini Card B for Wireless Testing		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 15 of 64	


NOTE: Supports only ADD2-N cards in this slot. ADD2-R cards are not supported.
NOTE: 12V MAX Icc = 2.1A
3.3V Max Icc = 3.0A
+V12S 5,17,31,33,35,45
R7B3
0.01_1%
SMR1206
V12S_SDVO
C7C1 22UF
C6B2 22UF
C7B1 22UF
C7B2 22UF
C7C4 0.1uF 10%
C7C2 0.1uF 10%
5..8,11,12,14,15,17,18,20..22,24,25,27,29,31,34,35,38,40,41,43..46,49..51,56..58
+V3.3S
R7C1
0.01_1%
SMR1206
V3.3S_SDVO
C7C6 100uF
C7C5 0.1uF 10%
C7C8 0.1uF 10%
J7C2
RST# 8,21,22,26,27,49,50
Key
SDVO_TVCLKIN 7
SDVO_TVCLKIN# 7
SDVO_INT 7
SDVO_INT# 7
SDVO_STALL 7
SDVO_STALL# 7
PCIE_X16
C35285-004
+V3.3S 5..8,11,12,14,15,17,18,20..22,24,25,27,29,31,34,35,38,40,41,43..46,49..51,56..58
R7C6
1M 5%
R7D2
1M 5%
7 SDVO_CTRLCLK
7 SDVO_CTRLDATA
7 SDVO_RED
7 SDVO_RED#
SDVO_REDP
SDVO_REDN
C7C9 0.1uF 10%
C7C10 0.1uF 10%
SDVO_REDP_C
SDVO_REDN_C
7 SDVO_GREEN
7 SDVO_GREEN#
SDVO_GREENP
SDVO_GREENN
C7C11 0.1uF 10%
C7C12 0.1uF 10%
SDVO_GREENP_C
SDVO_GREENN_C
7 SDVO_BLUE
7 SDVO_BLUE#
SDVO_BLUEP
SDVO_BLUEN
C7C13 0.1uF 10%
C7C14 0.1uF 10%
SDVO_BLUEP_C
SDVO_BLUEN_C
7 SDVO_CLK
7 SDVO_CLK#
SDVO_CLKP
SDVO_CLKN
C7D1 0.1uF 10%
C7D2 0.1uF 10%
SDVO_CLKP_C
SDVO_CLKN_C
NOTE: ADD2N CARD HAS P/U'S TO 2.5V. SCH INPUT IS 3.3V BUT CLAMPS TO 2.5V ANYWAY.
Crown Beach
Intel Confidential
Title
SDVO
Size A
Document Number
Rev 1.5
Date: Friday, November 16, 2007
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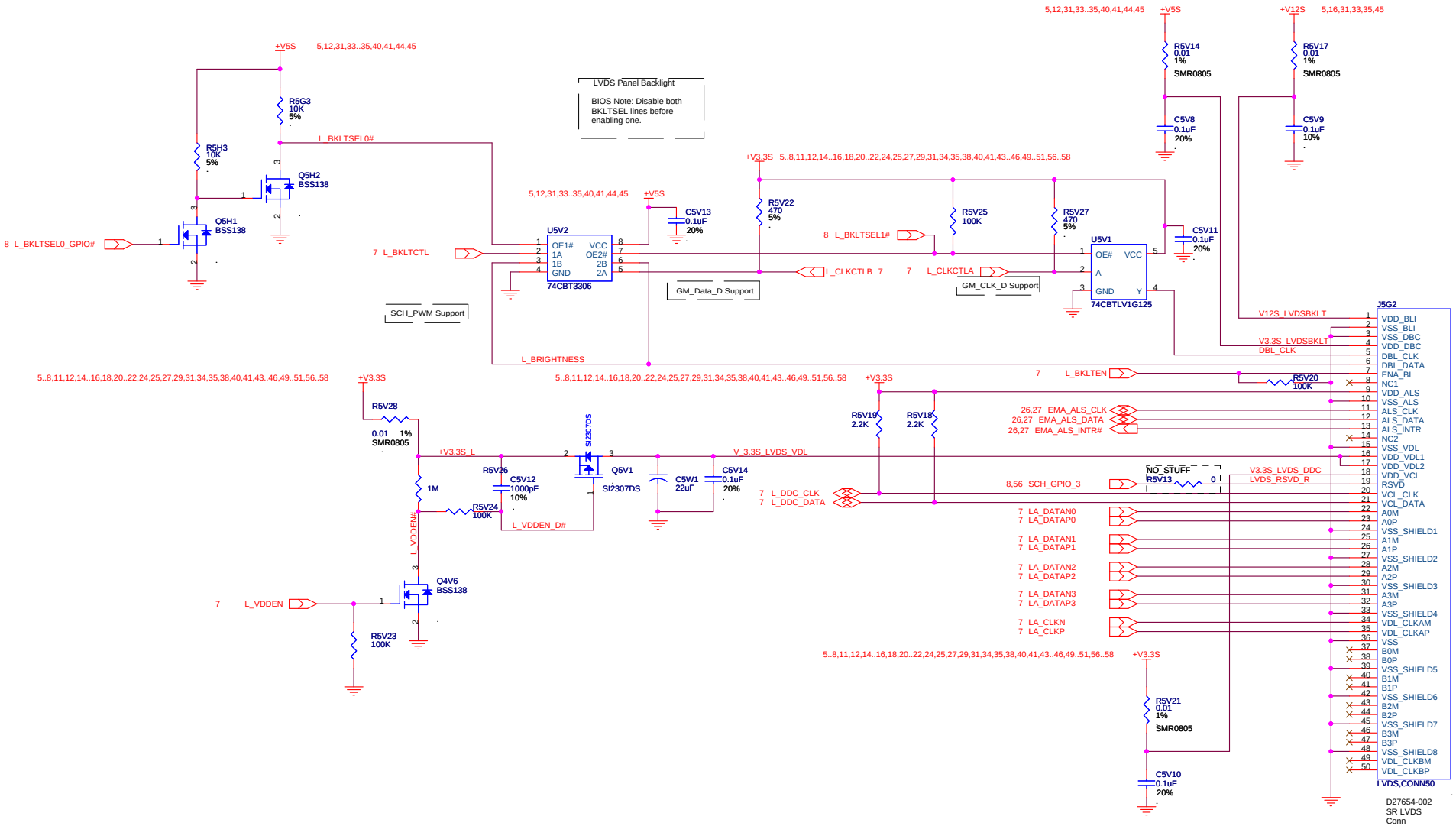
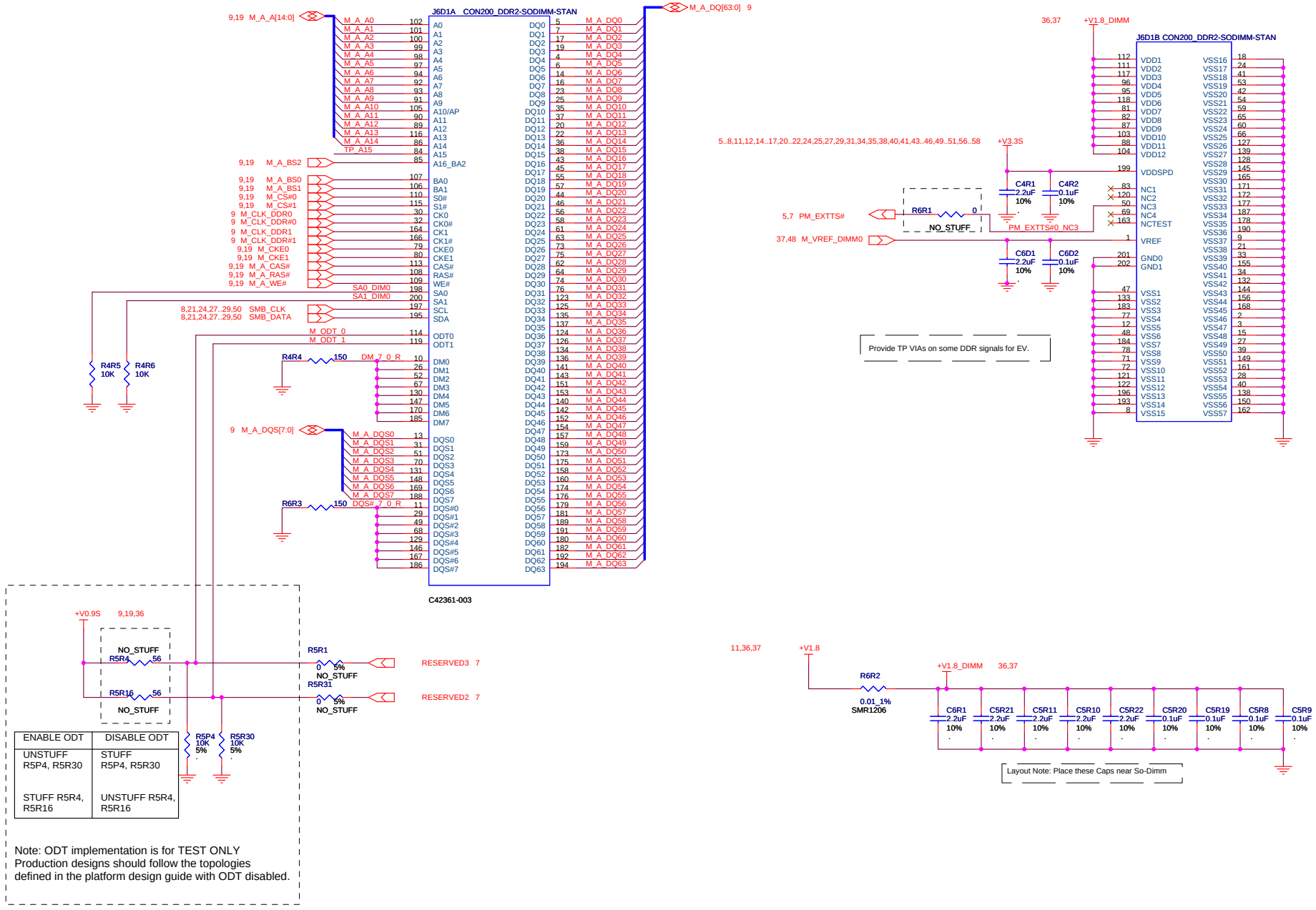
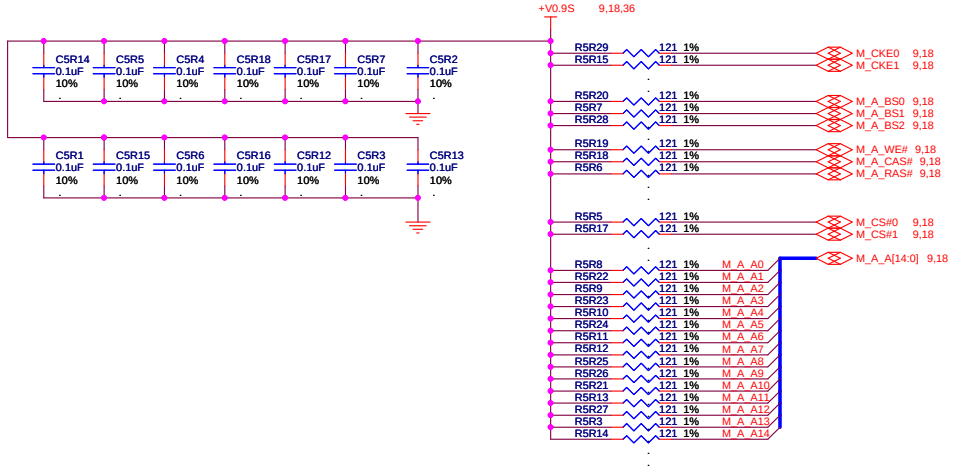


Crown Beach		Intel Confidential
Title: LVDS		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 17 of 64	

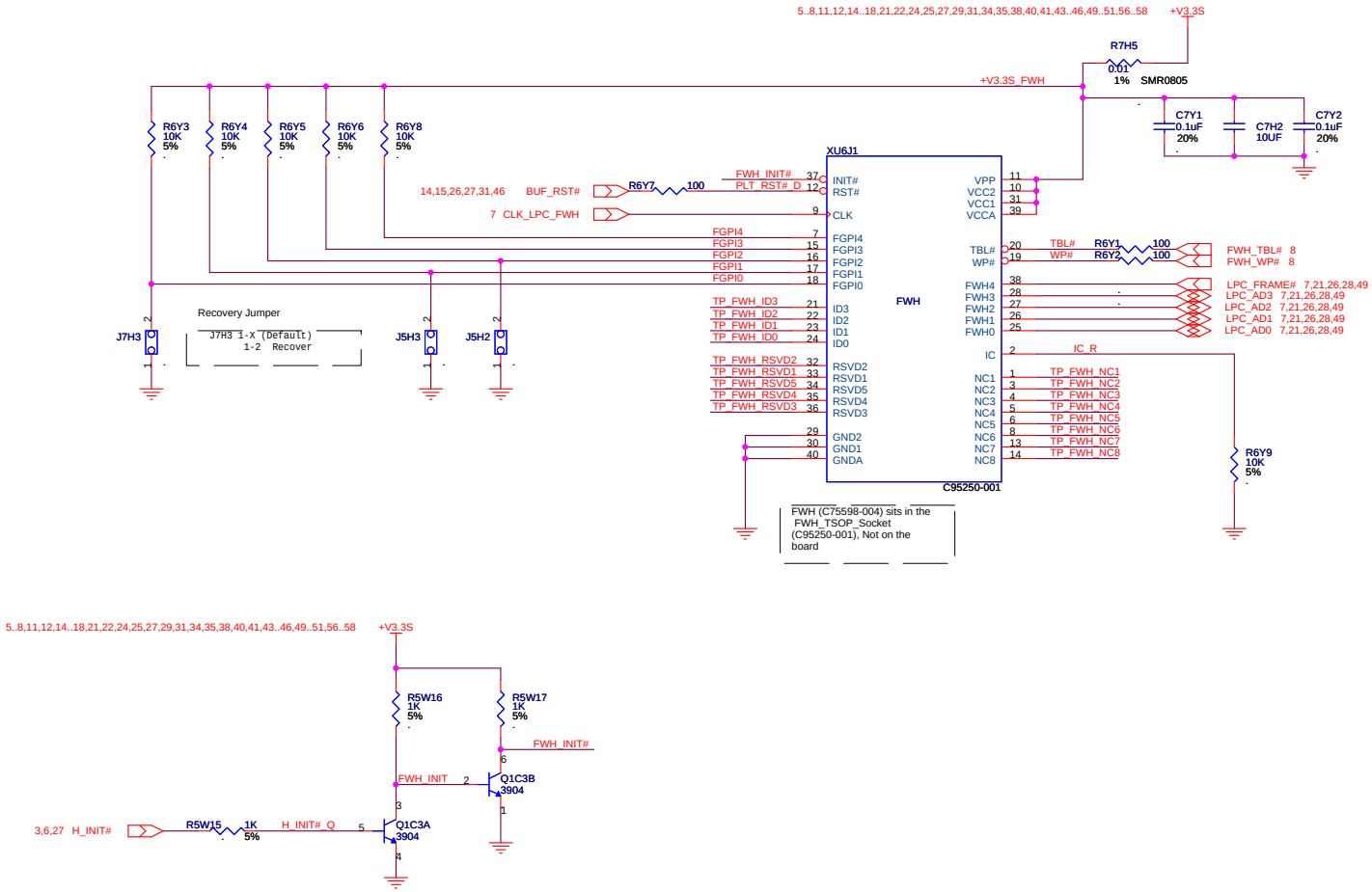


Crown Beach	Intel Confidential
Title: DDR2 SO-DIMM - Validation Only	
Size: A	Document Number:
Rev: 1.5	
Date: Friday, November 16, 2007	Sheet 18 of 64

Layout note: Place one cap close to every 2 pullup resistors terminated to +V0.9 and place it within 100 mils

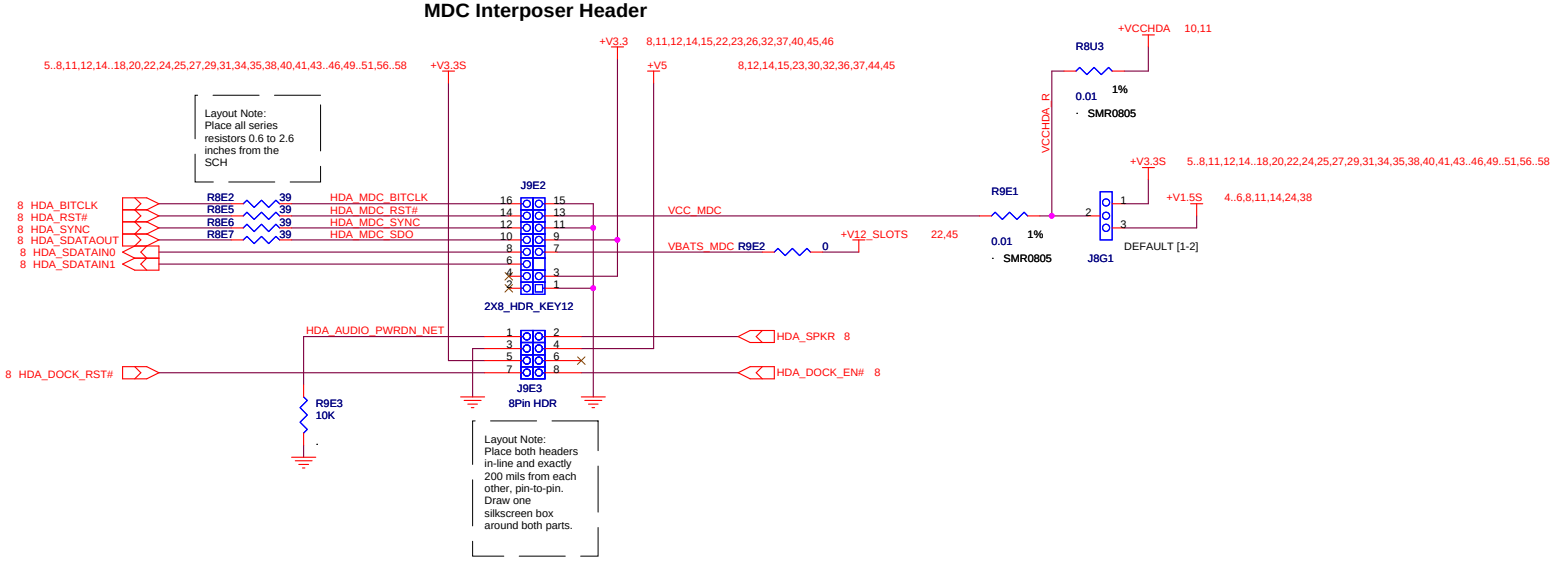


Crown Beach		Intel Confidential
Title: DDR2 Termination		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 19 of 64	



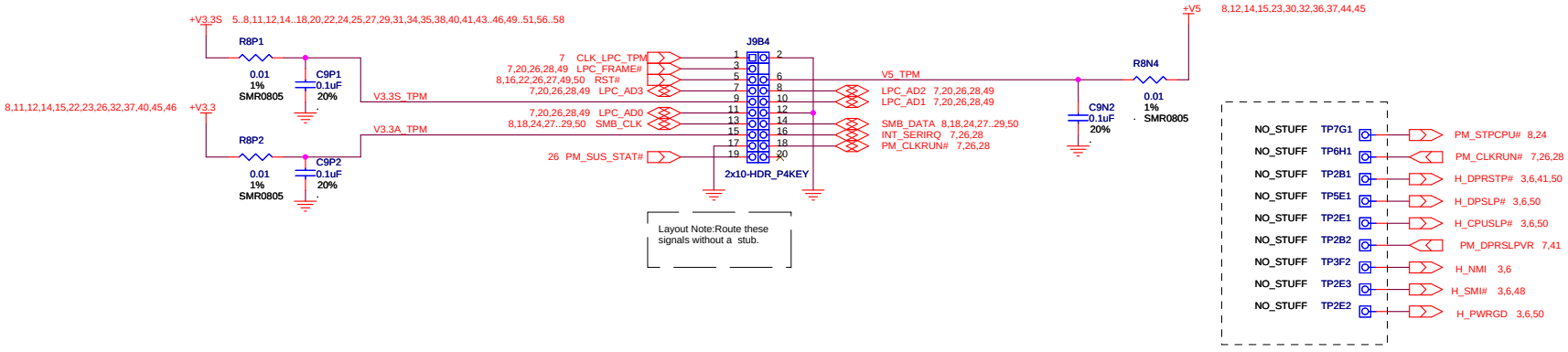
Crown Beach		Intel Confidential
Title: FWH		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 20 of 64	

MDC Interposer Header

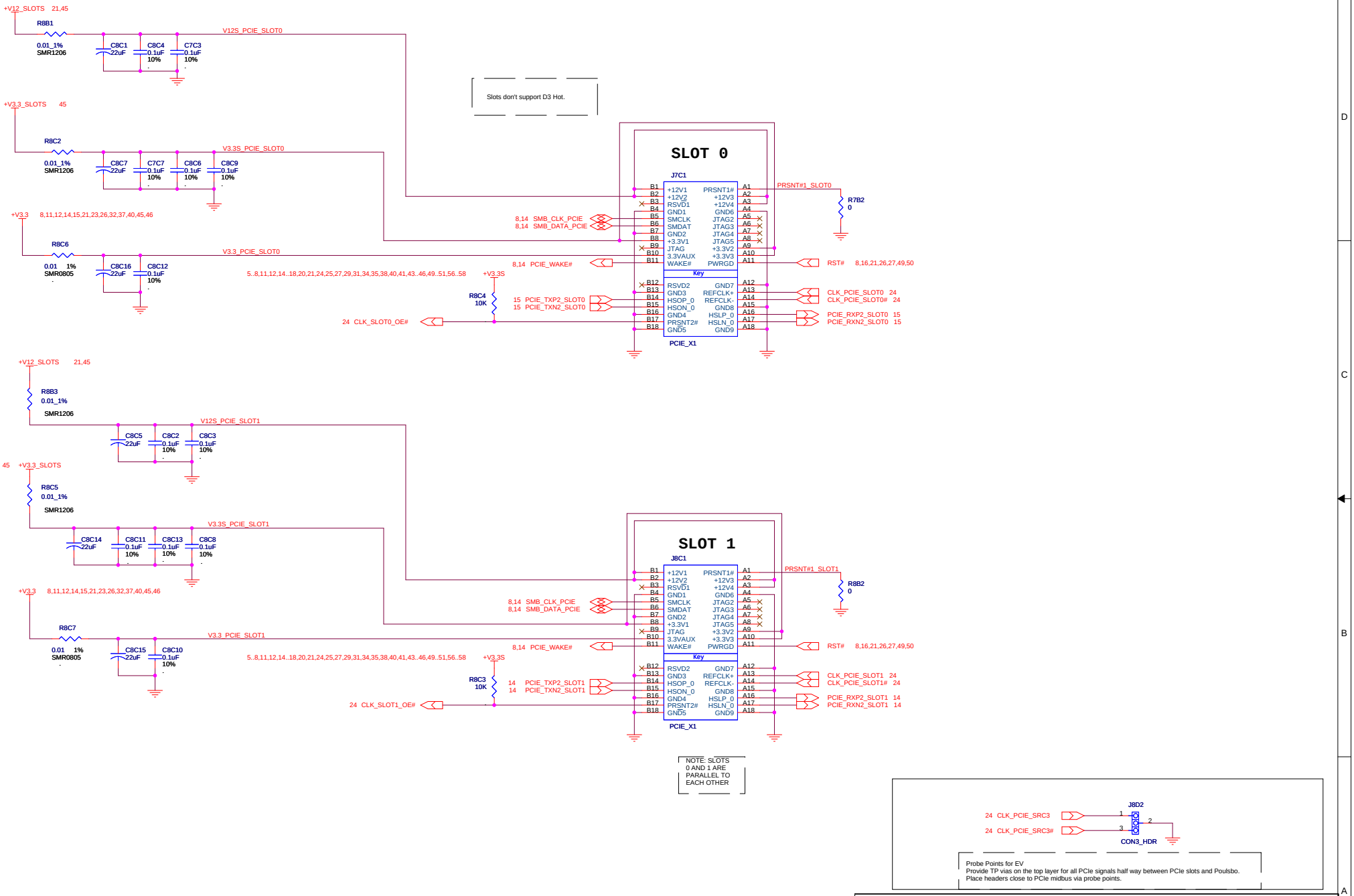


NOTE: Use the 2x8 part of the header to cable up to SDVO for HDMI capable ADD2N cards.

TPM HEADER



Crown Beach		Intel Confidential
Title: High Definitition Audio / TPM		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 21 of 64	


+V12_SLOTS 21,45
R8B1
0.01_1%
SMR1206
C8C1
22uF
C8C4
0.1uF
10%
C7C3
0.1uF
10%
V12S_PCIE_SLOT0
Slots don't support D3 Hot.
+V3.3_SLOTS 45
R8C2
0.01_1%
SMR1206
C8C7
22uF
C7C7
0.1uF
10%
C8C6
0.1uF
10%
C8C9
0.1uF
10%
V3.3S_PCIE_SLOT0
+V3.3 8,11,12,14,15,21,23,26,32,37,40,45,46
R8C6
0.01 1%
SMR0805
C8C16
22uF
C8C12
0.1uF
10%
V3.3_PCIE_SLOT0
SLOT 0
J7C1
PCIE_X1
PRSNT#1_SLOT0
R7B2
0
8,14 SMB_CLK_PCIE
8,14 SMB_DATA_PCIE
8,14 PCIE_WAKE#
RST# 8,16,21,26,27,49,50
5..8,11,12,14..18,20,21,24,25,27,29,31,34,35,38,40,41,43..46,49..51,56..58
+V3.3S
R8C4
10K
15 PCIE_TXP2_SLOT0
15 PCIE_TXN2_SLOT0
24 CLK_SLOT0_OE#
CLK_PCIE_SLOT0 24
CLK_PCIE_SLOT0# 24
PCIE_RXP2_SLOT0 15
PCIE_RXN2_SLOT0 15
+V12_SLOTS 21,45
R8B3
0.01_1%
SMR1206
C8C5
22uF
C8C2
0.1uF
10%
C8C3
0.1uF
10%
V12S_PCIE_SLOT1
45 +V3.3_SLOTS
R8C5
0.01_1%
SMR1206
C8C14
22uF
C8C11
0.1uF
10%
C8C13
0.1uF
10%
C8C8
0.1uF
10%
V3.3S_PCIE_SLOT1
+V3.3 8,11,12,14,15,21,23,26,32,37,40,45,46
R8C7
0.01 1%
SMR0805
C8C15
22uF
C8C10
0.1uF
10%
V3.3_PCIE_SLOT1
SLOT 1
J8C1
PCIE_X1
PRSNT#1_SLOT1
R8B2
0
8,14 SMB_CLK_PCIE
8,14 SMB_DATA_PCIE
8,14 PCIE_WAKE#
RST# 8,16,21,26,27,49,50
5..8,11,12,14..18,20,21,24,25,27,29,31,34,35,38,40,41,43..46,49..51,56..58
+V3.3S
R8C3
10K
14 PCIE_TXP2_SLOT1
14 PCIE_TXN2_SLOT1
24 CLK_SLOT1_OE#
CLK_PCIE_SLOT1 24
CLK_PCIE_SLOT1# 24
PCIE_RXP2_SLOT1 14
PCIE_RXN2_SLOT1 14
NOTE: SLOTS 0 AND 1 ARE PARALLEL TO EACH OTHER
24 CLK_PCIE_SRC3
24 CLK_PCIE_SRC3#
J8D2
CON3_HDR
Probe Points for EV
Provide TP vias on the top layer for all PCIe signals half way between PCIe slots and Poulsbo.
Place headers close to PCIe midbus via probe points.
Crown Beach
Intel Confidential
Title
PCI Express Slots
Size
Custom
Document Number
Rev
1.5
Date:
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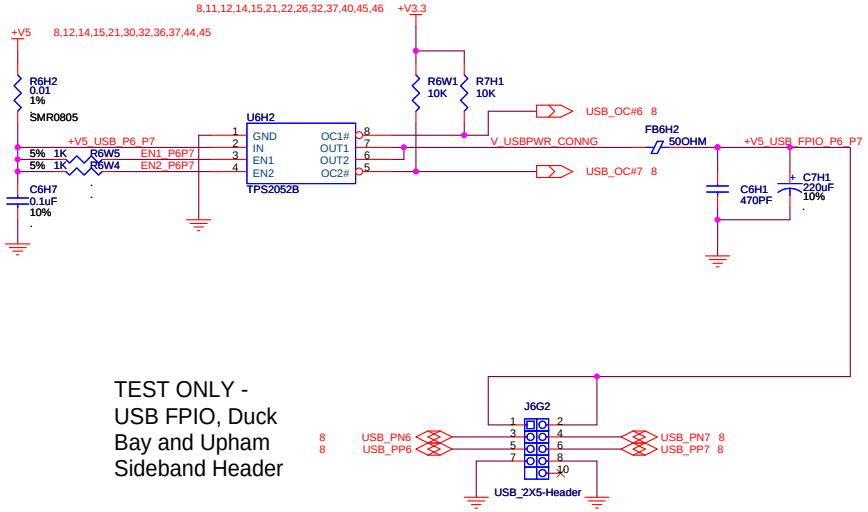
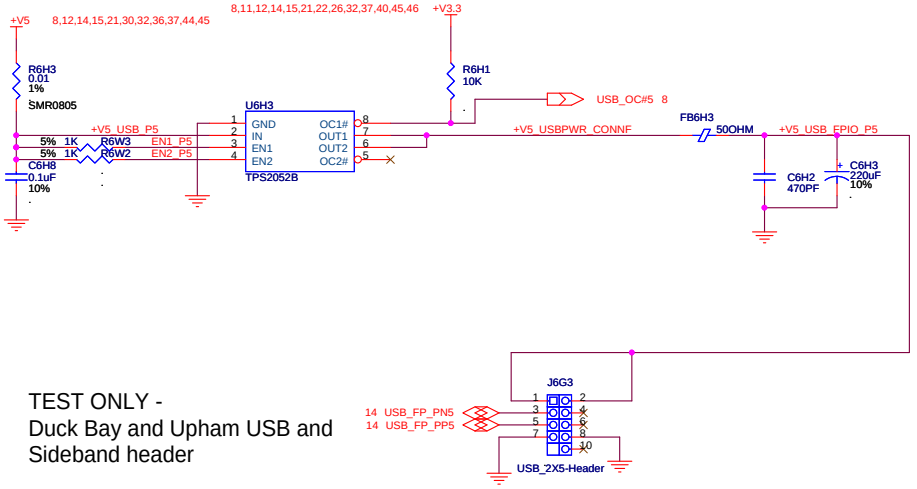
of
64





Crown Beach		Intel Confidential
Title: USB FPIO & Sideband		
Size: A	Document Number	Rev: 1.5
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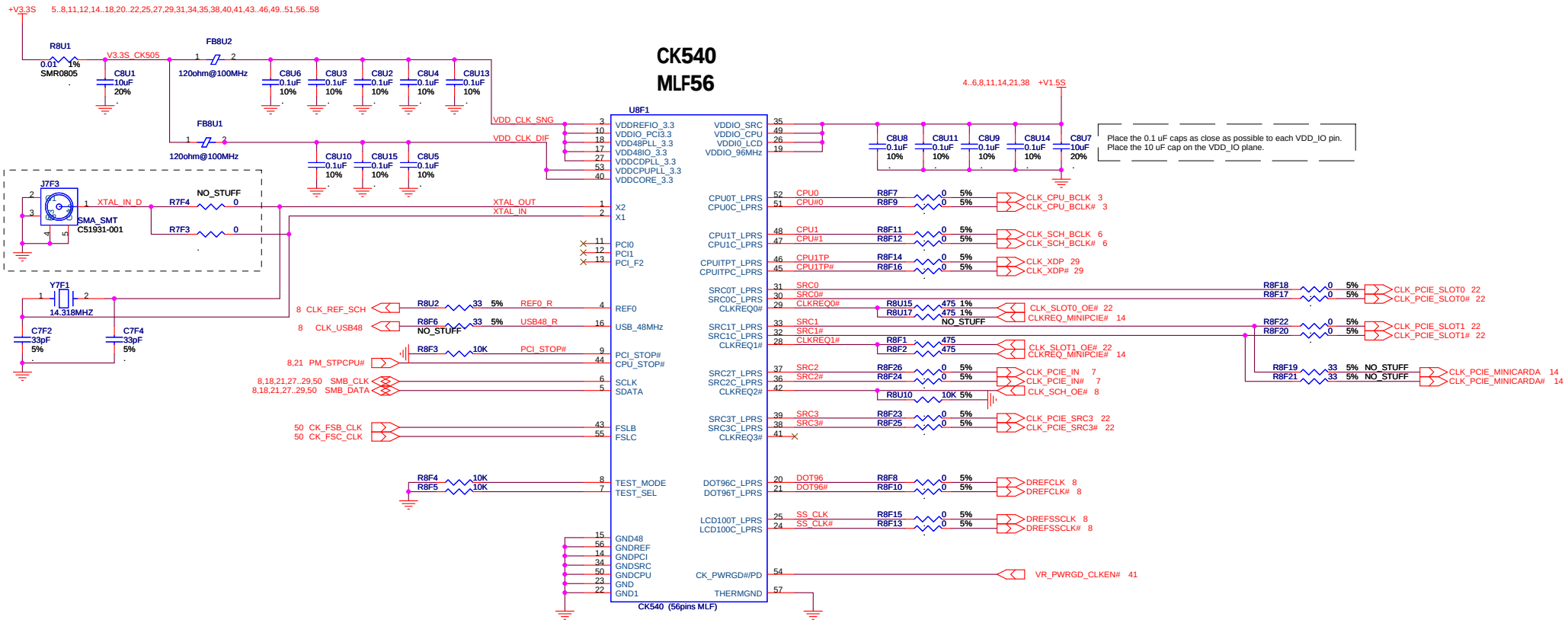
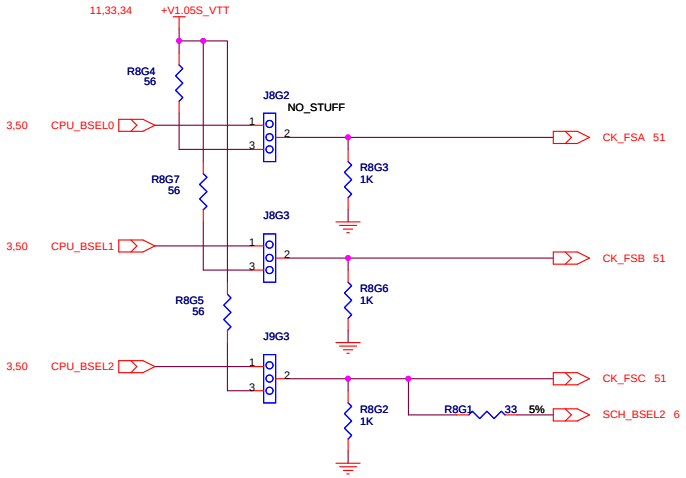
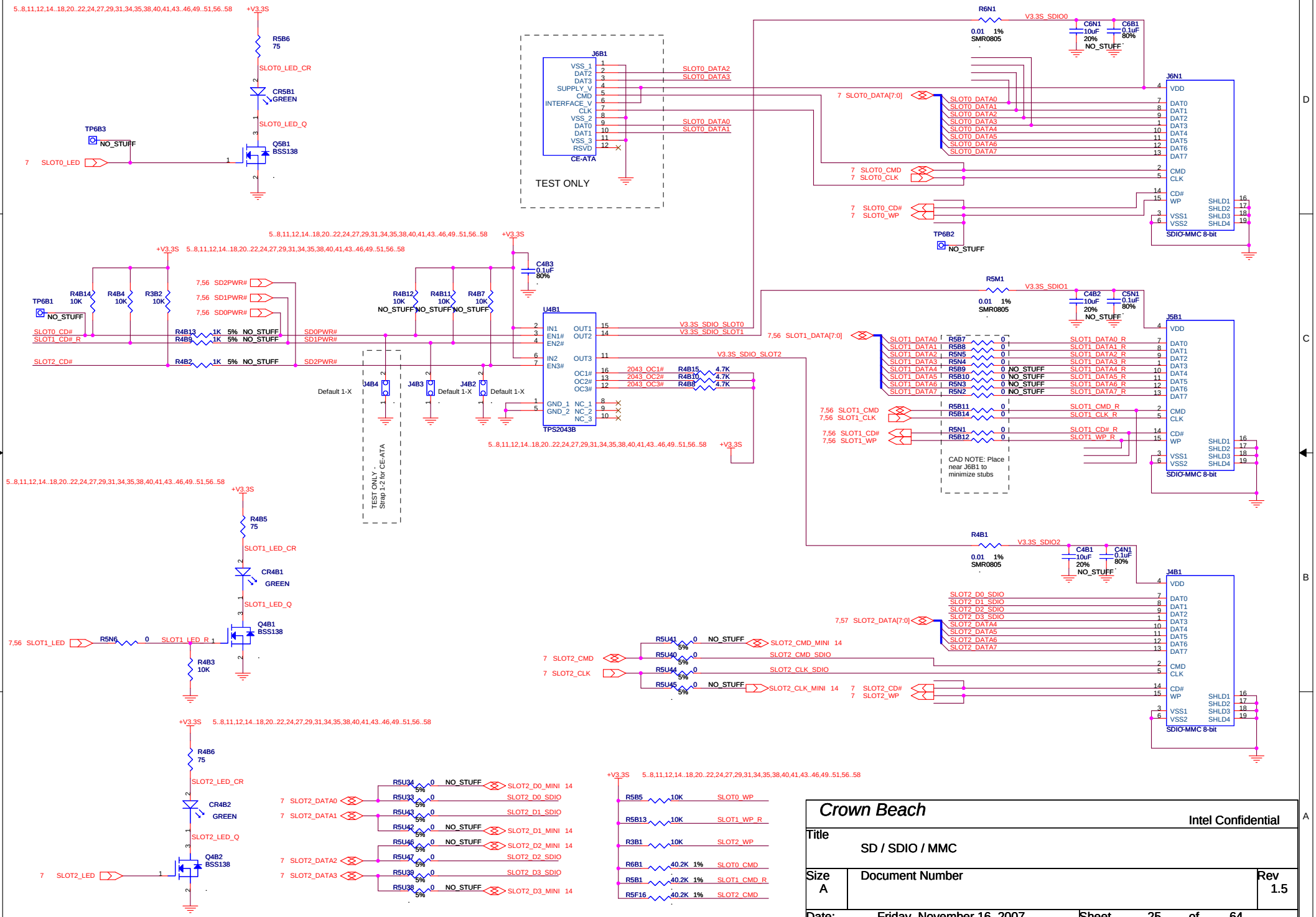




FSB Frequency Select:

FSB Freq (MHz)			
	CPU Driven (Default)	J8G3 -> 1 - 2 J9G3 -> 1 - 2	BSELS DRIVEN BY PROCESSOR
	400 (100 MHz host clk)	J8G3 -> Open J9G3 -> 2 - 3	CPU BSEL 1=0 CPU BSEL 2=1
	533 (133 MHz host clk)	J8G3 -> Open J9G3 -> Open	CPU BSEL 1=0 CPU BSEL 2=0

Crown Beach		Intel Confidential
Title: Clock CK540		
Size: A	Document Number	Rev: 1.5
Date: Friday, November 16, 2007	Sheet 24 of 64	


5..8,11,12,14..18,20..22,24,27,29,31,34,35,38,40,41,43..46,49..51,56..58
+V3.3S
R5B6
75
SLOT0_LED_CR
CR5B1
GREEN
SLOT0_LED_Q
Q5B1
BSS138
TP6B3
NO_STUFF
7 SLOT0_LED
J6B1
VSS_1
DAT2
DAT3
SUPPLY_V
CMD
INTERFACE_V
CLK
VSS_2
DAT0
DAT1
VSS_3
RSVD
CE-ATA
SLOT0_DATA2
SLOT0_DATA3
SLOT0_DATA0
SLOT0_DATA1
TEST ONLY
R6N1
V3.3S_SDIO0
0.01 1%
SMR0805
C6N1
10uF
20%
C6B1
0.1uF
80%
NO_STUFF
J6N1
7 SLOT0_DATA[7:0]
SLOT0_DATA0
SLOT0_DATA1
SLOT0_DATA2
SLOT0_DATA3
SLOT0_DATA4
SLOT0_DATA5
SLOT0_DATA6
SLOT0_DATA7
7 SLOT0_CMD
7 SLOT0_CLK
7 SLOT0_CD#
7 SLOT0_WP
TP6B2
NO_STUFF
VDD
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
CMD
CLK
CD#
WP
VSS1
VSS2
SHLD1
SHLD2
SHLD3
SHLD4
SDIO-MMC 8-bit
TP6B1
NO_STUFF
SLOT0_CD#
SLOT1_CD#_R
SLOT2_CD#
R4B14
10K
R4B4
10K
R3B2
10K
7,56 SD2PWR#
7,56 SD1PWR#
7,56 SD0PWR#
R4B13 1K 5% NO_STUFF
R4B9 1K 5% NO_STUFF
R4B2 1K 5% NO_STUFF
SD0PWR#
SD1PWR#
SD2PWR#
R4B12
10K
NO_STUFF
R4B11
10K
NO_STUFF
R4B7
10K
NO_STUFF
C4B3
0.1uF
80%
U4B1
IN1
EN1#
EN2#
IN2
EN3#
OUT1
OUT2
OUT3
OC1#
OC2#
OC3#
GND_1
GND_2
NC_1
NC_2
NC_3
TPS2043B
V3.3S_SDIO_SLOT0
V3.3S_SDIO_SLOT1
V3.3S_SDIO_SLOT2
2043_OC1#
2043_OC2#
2043_OC3#
R4B15 4.7K
R4B10 4.7K
R4B8 4.7K
J4B4
J4B3
J4B2
Default 1-X
TEST ONLY -
Strap 1-2 for CE-ATA
R5M1
V3.3S_SDIO1
C4B2
10uF
20%
C5N1
0.1uF
80%
J5B1
7,56 SLOT1_DATA[7:0]
SLOT1_DATA0
SLOT1_DATA1
SLOT1_DATA2
SLOT1_DATA3
SLOT1_DATA4
SLOT1_DATA5
SLOT1_DATA6
SLOT1_DATA7
R5B7 0
R5B8 0
R5N5 0
R5N4 0 NO_STUFF
R5B9 0 NO_STUFF
R5B10 0 NO_STUFF
R5N3 0 NO_STUFF
R5N2 0 NO_STUFF
SLOT1_DATA0_R
SLOT1_DATA1_R
SLOT1_DATA2_R
SLOT1_DATA3_R
SLOT1_DATA4_R
SLOT1_DATA5_R
SLOT1_DATA6_R
SLOT1_DATA7_R
7,56 SLOT1_CMD
7,56 SLOT1_CLK
R5B11 0
R5B14 0
SLOT1_CMD_R
SLOT1_CLK_R
7,56 SLOT1_CD#
7,56 SLOT1_WP
R5N1 0
R5B12 0
SLOT1_CD#_R
SLOT1_WP_R
CAD NOTE: Place near J6B1 to minimize stubs
5..8,11,12,14..18,20..22,24,27,29,31,34,35,38,40,41,43..46,49..51,56..58
+V3.3S
R4B5
75
SLOT1_LED_CR
CR4B1
GREEN
SLOT1_LED_Q
Q4B1
BSS138
7,56 SLOT1_LED
R5N6 0 SLOT1_LED_R
R4B3
10K
R4B1
V3.3S_SDIO2
C4B1
10uF
20%
C4N1
0.1uF
80%
J4B1
7,57 SLOT2_DATA[7:0]
SLOT2_D0_SDIO
SLOT2_D1_SDIO
SLOT2_D2_SDIO
SLOT2_D3_SDIO
SLOT2_DATA4
SLOT2_DATA5
SLOT2_DATA6
SLOT2_DATA7
R5U41 0 NO_STUFF SLOT2_CMD_MINI 14
R5U40 0 SLOT2_CMD_SDIO
R5U44 0 SLOT2_CLK_SDIO
R5U45 0 NO_STUFF SLOT2_CLK_MINI 14
7 SLOT2_CMD
7 SLOT2_CLK
7 SLOT2_CD#
7 SLOT2_WP
R4B6
75
SLOT2_LED_CR
CR4B2
GREEN
SLOT2_LED_Q
Q4B2
BSS138
7 SLOT2_LED
7 SLOT2_DATA0
7 SLOT2_DATA1
7 SLOT2_DATA2
7 SLOT2_DATA3
R5U34 0 NO_STUFF SLOT2_D0_MINI 14
R5U33 0 SLOT2_D0_SDIO
R5U43 0 SLOT2_D1_SDIO
R5U42 0 NO_STUFF SLOT2_D1_MINI 14
R5U46 0 NO_STUFF SLOT2_D2_MINI 14
R5U47 0 SLOT2_D2_SDIO
R5U39 0 SLOT2_D3_SDIO
R5U38 0 NO_STUFF SLOT2_D3_MINI 14
R5B5 10K SLOT0_WP
R5B13 10K SLOT1_WP_R
R3B1 10K SLOT2_WP
R6B1 40.2K 1% SLOT0_CMD
R5B1 40.2K 1% SLOT1_CMD_R
R5F16 40.2K 1% SLOT2_CMD
Crown Beach
Intel Confidential
Title
SD / SDIO / MMC
Size
A
Document Number
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1.5
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Boot Mode Programming Straps

P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. System needs to supply +V3.3A to flash connector.

MODE TYPE	MD0	MD1	MD2	NMI(P29)
Run Mode	0	0	1	0
Program Boot Block	0	0	1	1

NOTE:GND_SYS_ISENSE tie to GND is on Page 53

NOTE: Place C7T1 decoupling cap close to VCL pin 13

EC RST# Jumper
J7E2 1-2 (Default)
J7E2 2-3 (H8 held in reset)

J8E2 1-2 (Default)
J8E3 1-2 (Default)

J8E5 1-X (Default)

J8E4 1-X (Default)

NOTE: Stuff R7T17 for write protect

H8S/2117 TFP144

D96714-001

Backup option in case of 2104 sub

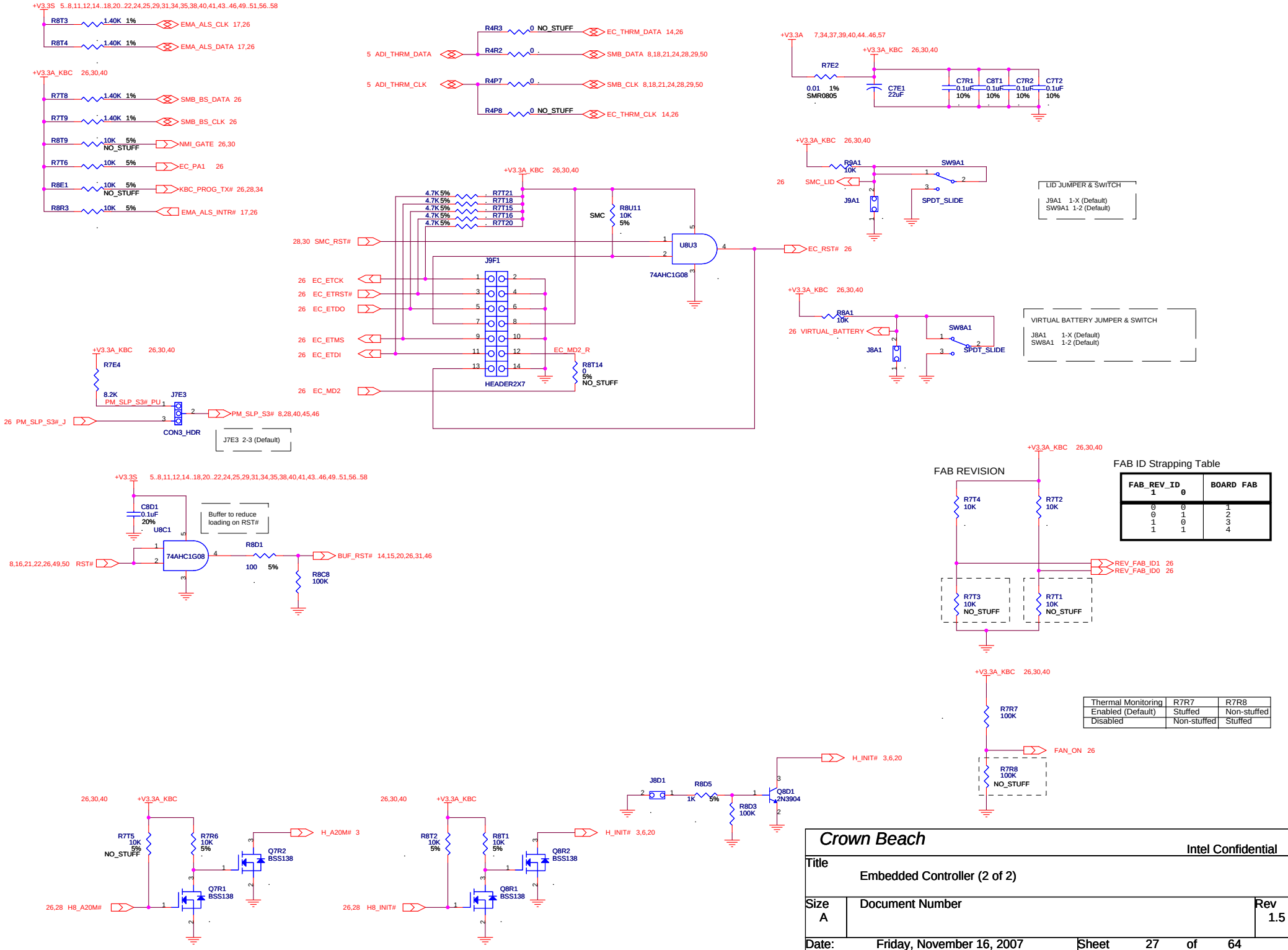
Optional SPI Flash for testing only

SST SPI FLASH NO_STUFF

H8 JTAG

J8E1 1-X (Default)

Crown Beach	Intel Confidential
Title: Embedded Controller (1 of 2)	
Size: A	Document Number:
Rev: 1.5	
Date: Friday, November 16, 2007	Sheet 26 of 64


+V3.3S 5..8,11,12,14..18,20..22,24,25,29,31,34,35,38,40,41,43..46,49..51,56..58
R8T3 1.40K 1% EMA_ALS_CLK 17,26
R8T4 1.40K 1% EMA_ALS_DATA 17,26
+V3.3A_KBC 26,30,40
R7T8 1.40K 1% SMB_BS_DATA 26
R7T9 1.40K 1% SMB_BS_CLK 26
R8T9 10K 5% NO_STUFF NMI_GATE 26,30
R7T6 10K 5% EC_PA1 26
R8E1 10K 5% NO_STUFF KBC_PROG_TX# 26,28,34
R8R3 10K 5% EMA_ALS_INTR# 17,26
5 ADI_THRM_DATA
R4R3 0 NO_STUFF EC_THRM_DATA 14,26
R4R2 0 SMB_DATA 8,18,21,24,28,29,50
5 ADI_THRM_CLK
R4P7 0 SMB_CLK 8,18,21,24,28,29,50
R4P8 0 NO_STUFF EC_THRM_CLK 14,26
+V3.3A 7,34,37,39,40,44..46,57
+V3.3A_KBC 26,30,40
R7E2 0.01 1% SMR0805
C7E1 22uF
C7R1 0.1uF 10%
C8T1 0.1uF 10%
C7R2 0.1uF 10%
C7T2 0.1uF 10%
+V3.3A_KBC 26,30,40
R9A1 10K
26 SMC_LID
J9A1
SW9A1
SPDT_SLIDE
LID JUMPER & SWITCH
J9A1 1-X (Default)
SW9A1 1-2 (Default)
+V3.3A_KBC 26,30,40
4.7K 5% R7T21
4.7K 5% R7T18
4.7K 5% R7T15
4.7K 5% R7T16
4.7K 5% R7T20
SMC
R8U11 10K 5%
28,30 SMC_RST#
U8U3
74AHC1G08
EC_RST# 26
J9F1
26 EC_ETCK
26 EC_ETRST#
26 EC_ETDO
26 EC_ETMS
26 EC_ETDI
26 EC_MD2
EC_MD2_R
R8T14 0 5% NO_STUFF
HEADER2X7
+V3.3A_KBC 26,30,40
R8A1 10K
26 VIRTUAL_BATTERY
J8A1
SW8A1
SPDT_SLIDE
VIRTUAL BATTERY JUMPER & SWITCH
J8A1 1-X (Default)
SW8A1 1-2 (Default)
+V3.3A_KBC 26,30,40
R7E4 8.2K
PM_SLP_S3#_PU
J7E3
26 PM_SLP_S3#_J
PM_SLP_S3# 8,28,40,45,46
CON3_HDR
J7E3 2-3 (Default)
+V3.3S 5..8,11,12,14..18,20..22,24,25,29,31,34,35,38,40,41,43..46,49..51,56..58
C8D1 0.1uF 20%
U8C1
Buffer to reduce loading on RST#
8,16,21,22,26,49,50 RST#
74AHC1G08
R8D1 100 5%
R8C8 100K
BUF_RST# 14,15,20,26,31,46
+V3.3A_KBC 26,30,40
FAB REVISION
R7T4 10K
R7T2 10K
REV_FAB_ID1 26
REV_FAB_ID0 26
R7T3 10K NO_STUFF
R7T1 10K NO_STUFF
FAB ID Strapping Table
FAB_REV_ID 1 0 | BOARD FAB
0 0 | 1
0 1 | 2
1 0 | 3
1 1 | 4
+V3.3A_KBC 26,30,40
R7R7 100K
FAN_ON 26
R7R8 100K NO_STUFF
Thermal Monitoring | R7R7 | R7R8
Enabled (Default) | Stuffed | Non-stuffed
Disabled | Non-stuffed | Stuffed
H_INIT# 3,6,20
J8D1
R8D5 1K 5%
R8D3 100K
Q8D1 2N3904
26,30,40 +V3.3A_KBC
R7T5 10K 5% NO_STUFF
R7R6 10K 5%
Q7R2 BSS138
H_A20M# 3
Q7R1 BSS138
26,28 H8_A20M#
26,30,40 +V3.3A_KBC
R8T2 10K 5%
R8T1 10K 5%
Q8R2 BSS138
H_INIT# 3,6,20
Q8R1 BSS138
26,28 H8_INIT#
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Embedded Controller (2 of 2)
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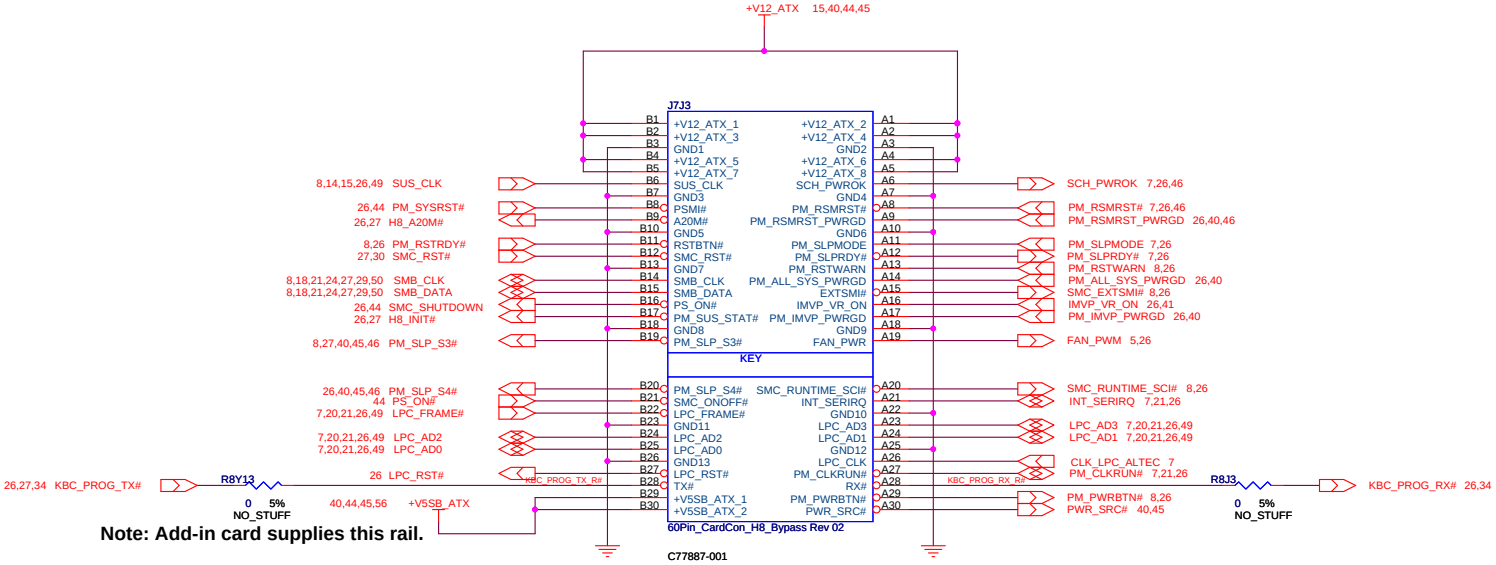
Note: Add-in card supplies this rail.



Note: Add-in card supplies this rail.

Note: Model has been changed from original.
Pin definition is different

Crown Beach		Intel Confidential
Title: Embedded Controller Bypass		
Size: A	Document Number	Rev: 1.5
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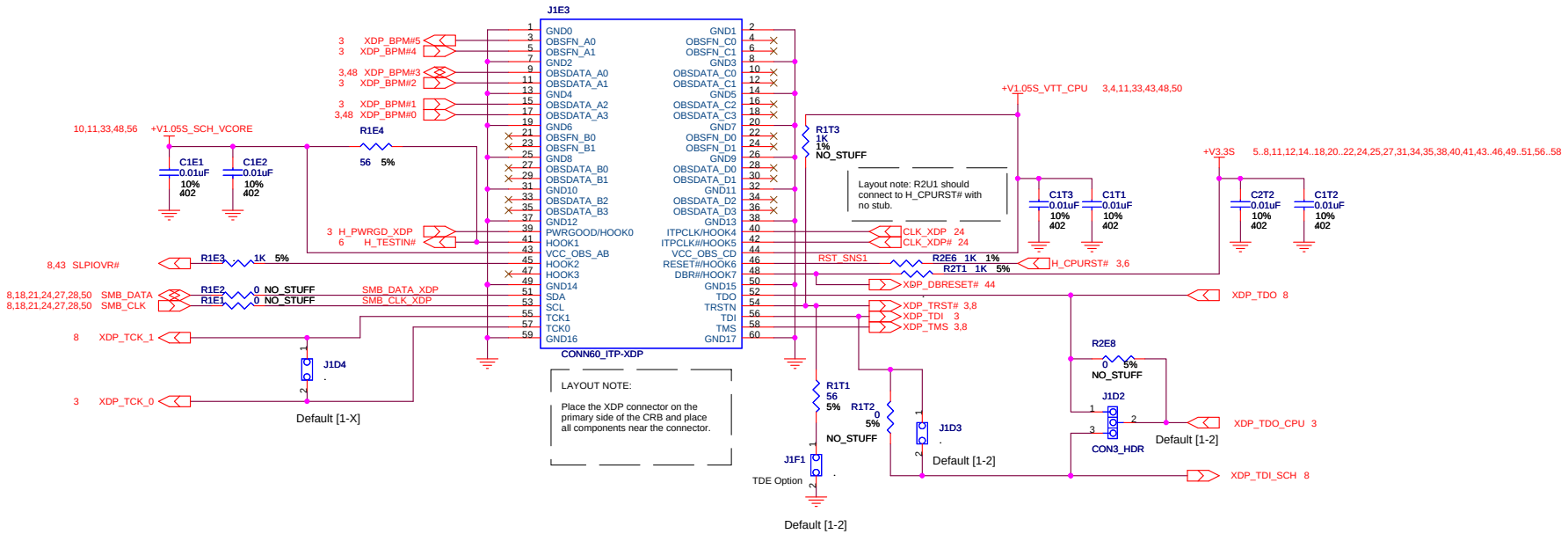
XDP



Crown Beach		Intel Confidential
Title: XDP		
Size: A	Document Number	Rev: 1.5
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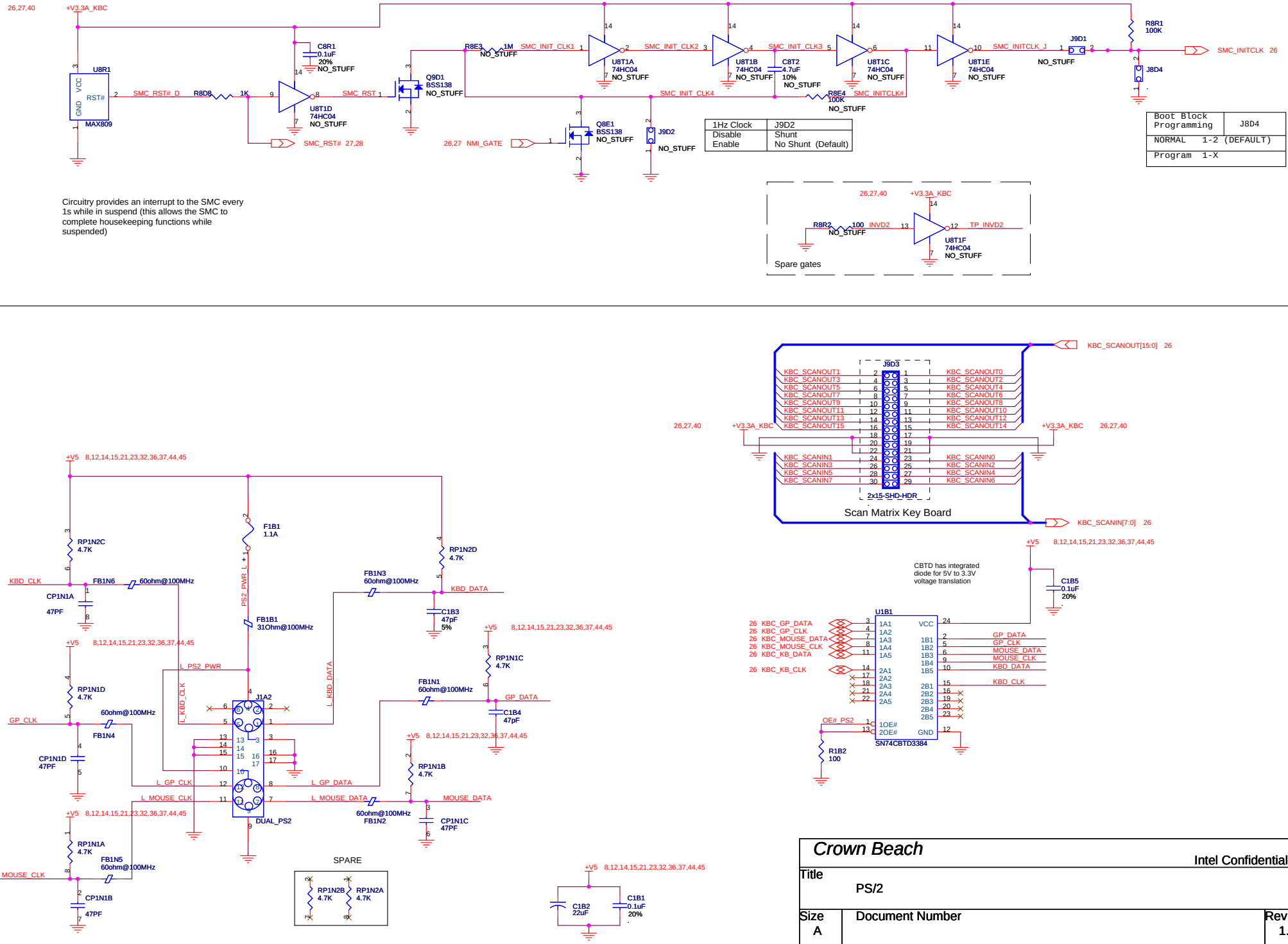
26,27,40
+V3.3A_KBC
U8R1
VCC
RST#
GND
MAX809
SMC_RST# D
R8D8
1K
C8R1
0.1uF
20%
NO_STUFF
U8T1D
74HC04
NO_STUFF
SMC_RST
SMC_RST# 27,28
Q9D1
BSS138
NO_STUFF
R8E3
1M
NO_STUFF
SMC_INIT_CLK1
U8T1A
74HC04
NO_STUFF
SMC_INIT_CLK2
U8T1B
74HC04
NO_STUFF
C8T2
4.7uF
10%
NO_STUFF
SMC_INIT_CLK3
U8T1C
74HC04
NO_STUFF
U8T1E
74HC04
NO_STUFF
SMC_INITCLK_J
J9D1
NO_STUFF
R8R1
100K
SMC_INITCLK 26
J8D4
SMC_INIT_CLK4
R8E4
100K
NO_STUFF
SMC_INITCLK#
26,27 NMI_GATE
Q8E1
BSS138
NO_STUFF
J9D2
NO_STUFF
1Hz Clock Disable Enable
J9D2 Shunt No Shunt (Default)
Boot Block Programming
J8D4
NORMAL 1-2 (DEFAULT)
Program 1-X
Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)
26,27,40
+V3.3A_KBC
R8R2
100
NO_STUFF
INVD2
U8T1F
74HC04
NO_STUFF
TP_INVD2
Spare gates
KBC_SCANOUT[15:0] 26
J9D3
KBC_SCANOUT1
KBC_SCANOUT3
KBC_SCANOUT5
KBC_SCANOUT7
KBC_SCANOUT9
KBC_SCANOUT11
KBC_SCANOUT13
KBC_SCANOUT15
KBC_SCANOUT0
KBC_SCANOUT2
KBC_SCANOUT4
KBC_SCANOUT6
KBC_SCANOUT8
KBC_SCANOUT10
KBC_SCANOUT12
KBC_SCANOUT14
KBC_SCANIN1
KBC_SCANIN3
KBC_SCANIN5
KBC_SCANIN7
KBC_SCANIN0
KBC_SCANIN2
KBC_SCANIN4
KBC_SCANIN6
2x15-SHD-HDR
Scan Matrix Key Board
KBC_SCANIN[7:0] 26
+V5 8,12,14,15,21,23,32,36,37,44,45
RP1N2C
4.7K
KBD_CLK
FB1N6
60ohm@100MHz
CP1N1A
47PF
F1B1
1.1A
PS2_PWR
FB1B1
31Ohm@100MHz
RP1N2D
4.7K
FB1N3
60ohm@100MHz
KBD_DATA
C1B3
47PF
5%
RP1N1C
4.7K
FB1N1
60ohm@100MHz
GP_DATA
C1B4
47pF
RP1N1D
4.7K
GP_CLK
FB1N4
CP1N1D
47PF
L_PS2_PWR
L_KBD_CLK
L_KBD_DATA
L_GP_CLK
L_GP_DATA
L_MOUSE_CLK
L_MOUSE_DATA
J1A2
DUAL_PS2
RP1N1B
4.7K
MOUSE_DATA
FB1N2
60ohm@100MHz
CP1N1C
47PF
RP1N1A
4.7K
FB1N5
60ohm@100MHz
MOUSE_CLK
CP1N1B
47PF
SPARE
RP1N2B
4.7K
RP1N2A
4.7K
C1B2
22uF
C1B1
0.1uF
20%
CBTD has integrated diode for 5V to 3.3V voltage translation
U1B1
SN74CBTD3384
26 KBC_GP_DATA
26 KBC_GP_CLK
26 KBC_MOUSE_DATA
26 KBC_MOUSE_CLK
26 KBC_KB_DATA
26 KBC_KB_CLK
GP_DATA
GP_CLK
MOUSE_DATA
MOUSE_CLK
KBD_DATA
KBD_CLK
OE# PS2
R1B2
100
C1B5
0.1uF
20%
Crown Beach
Intel Confidential
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PS/2
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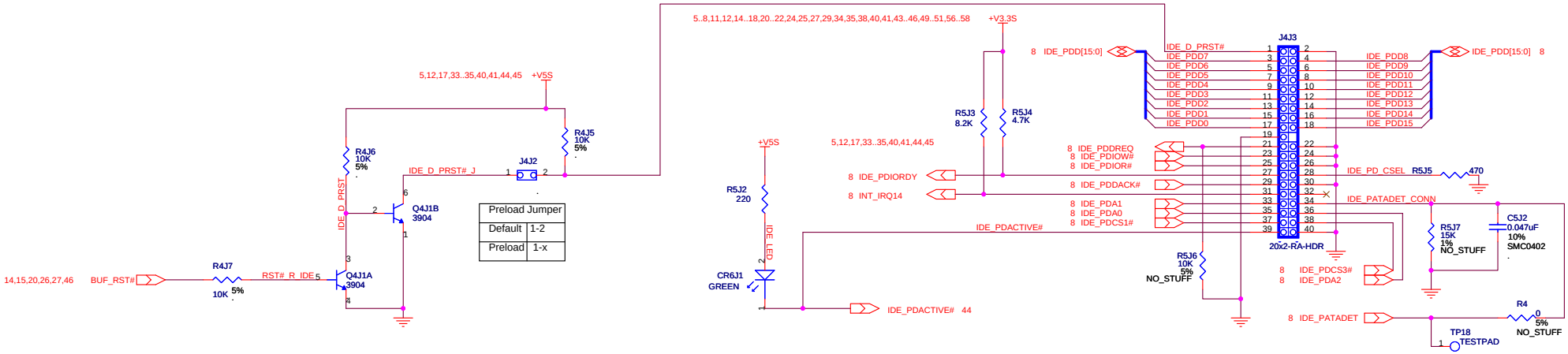
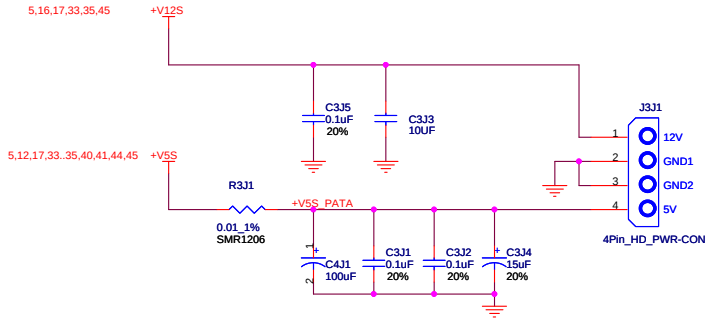


OUTPUT ONLY
DO NOT PLUG ATX POWER SUPPLY HARD
DRIVE POWER CONNECTORS INTO THIS CONNECTOR!!!!!!!



Crown Beach			Intel Confidential
Title: PATA			
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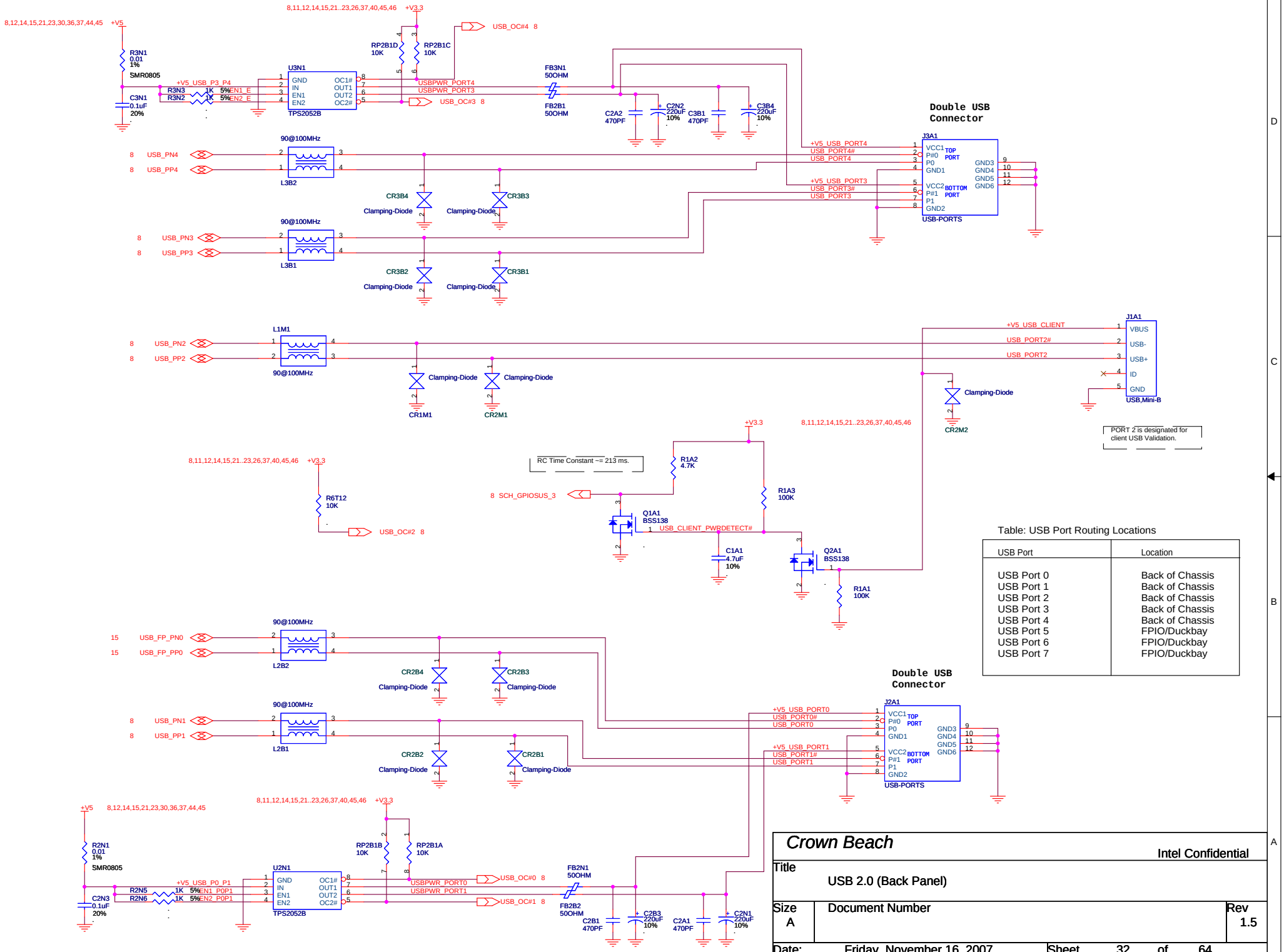

Table: USB Port Routing Locations

USB Port	Location
USB Port 0	Back of Chassis
USB Port 1	Back of Chassis
USB Port 2	Back of Chassis
USB Port 3	Back of Chassis
USB Port 4	Back of Chassis
USB Port 5	FPIO/Duckbay
USB Port 6	FPIO/Duckbay
USB Port 7	FPIO/Duckbay

Crown Beach

Intel Confidential

Title: USB 2.0 (Back Panel)

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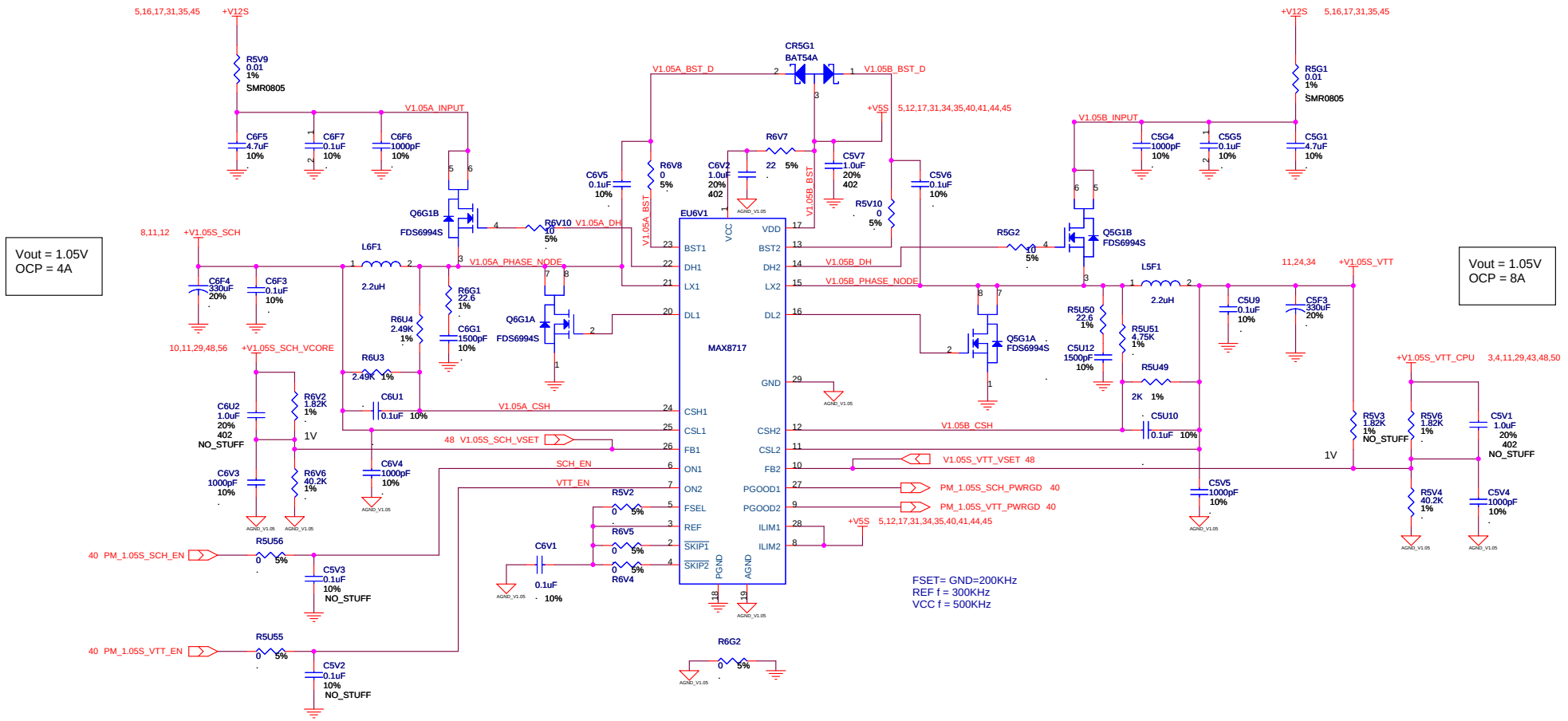

Crown Beach		Intel Confidential
Title: Dual 1.05V VR		
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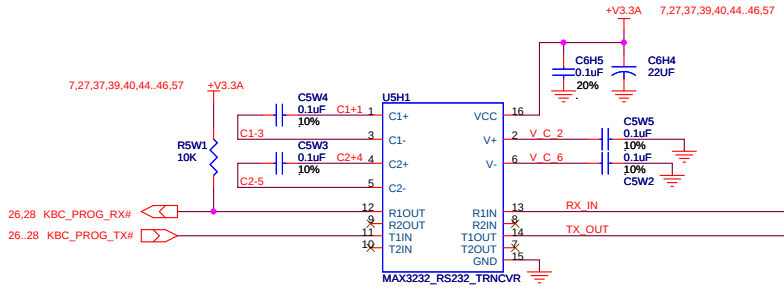
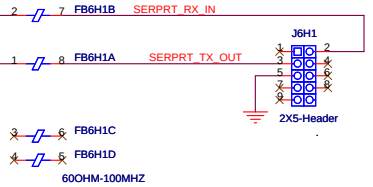
RS-232 TRANSCEIVER

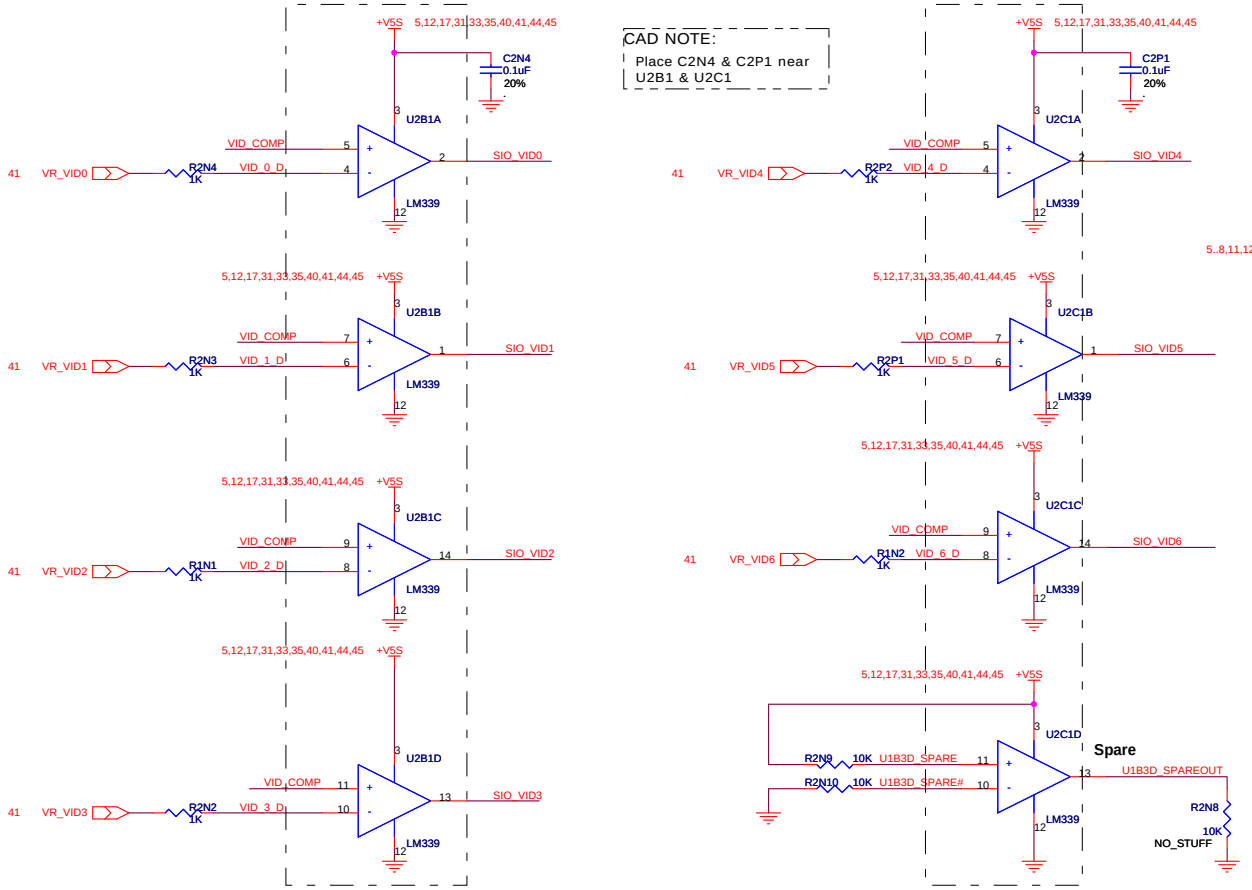


SERIAL PORT CONNECTOR

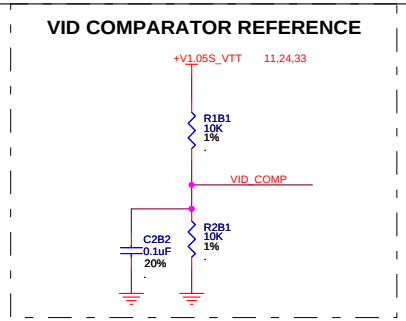


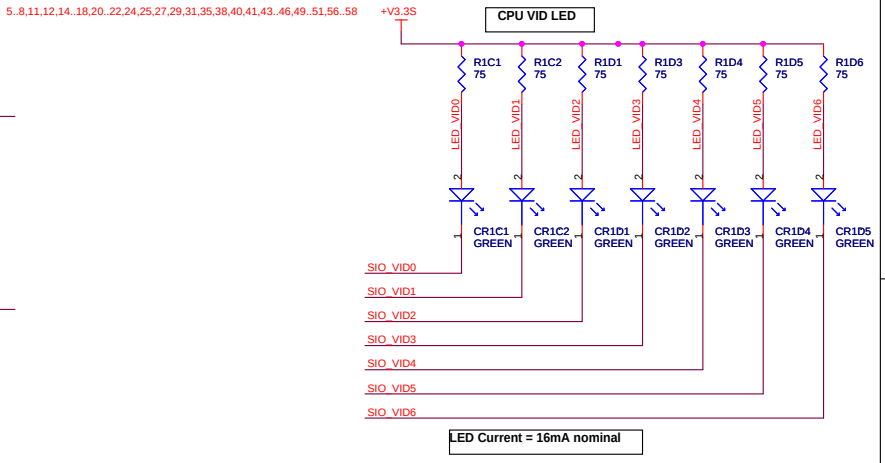
NOTE: USED FOR FACTORY PROGRAMMING OF EMBEDDED CONTROLLER

SIO VID VOLTAGE TRANSLATION



VID COMPARATOR REFERENCE





Crown Beach		Intel Confidential
Title: Legacy Support		
Size: A	Document Number	Rev: 1.5
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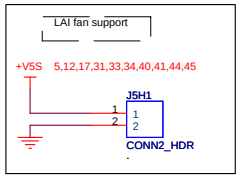
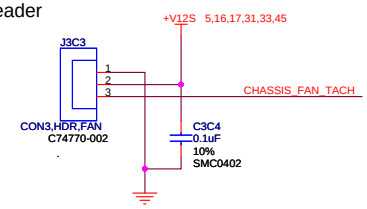
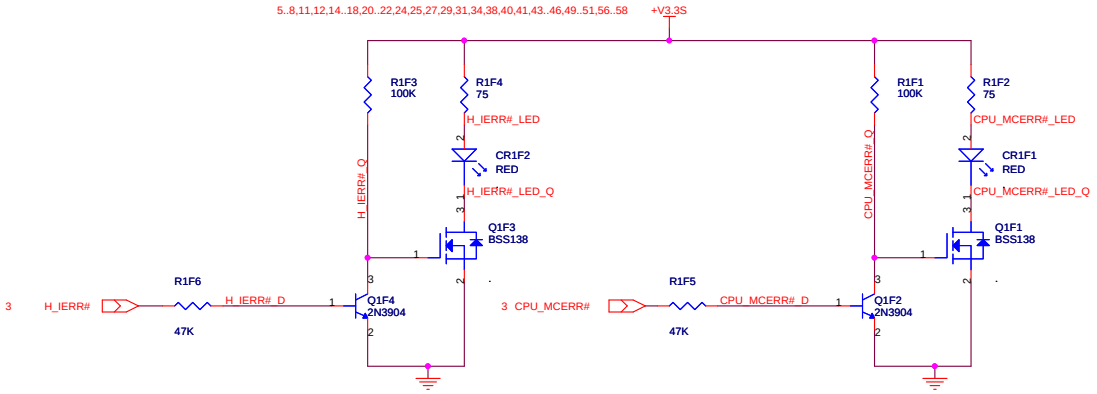


Chassis Fan Header





Crown Beach		Intel Confidential
Title: LAI Fan Support - Debug LEDs		
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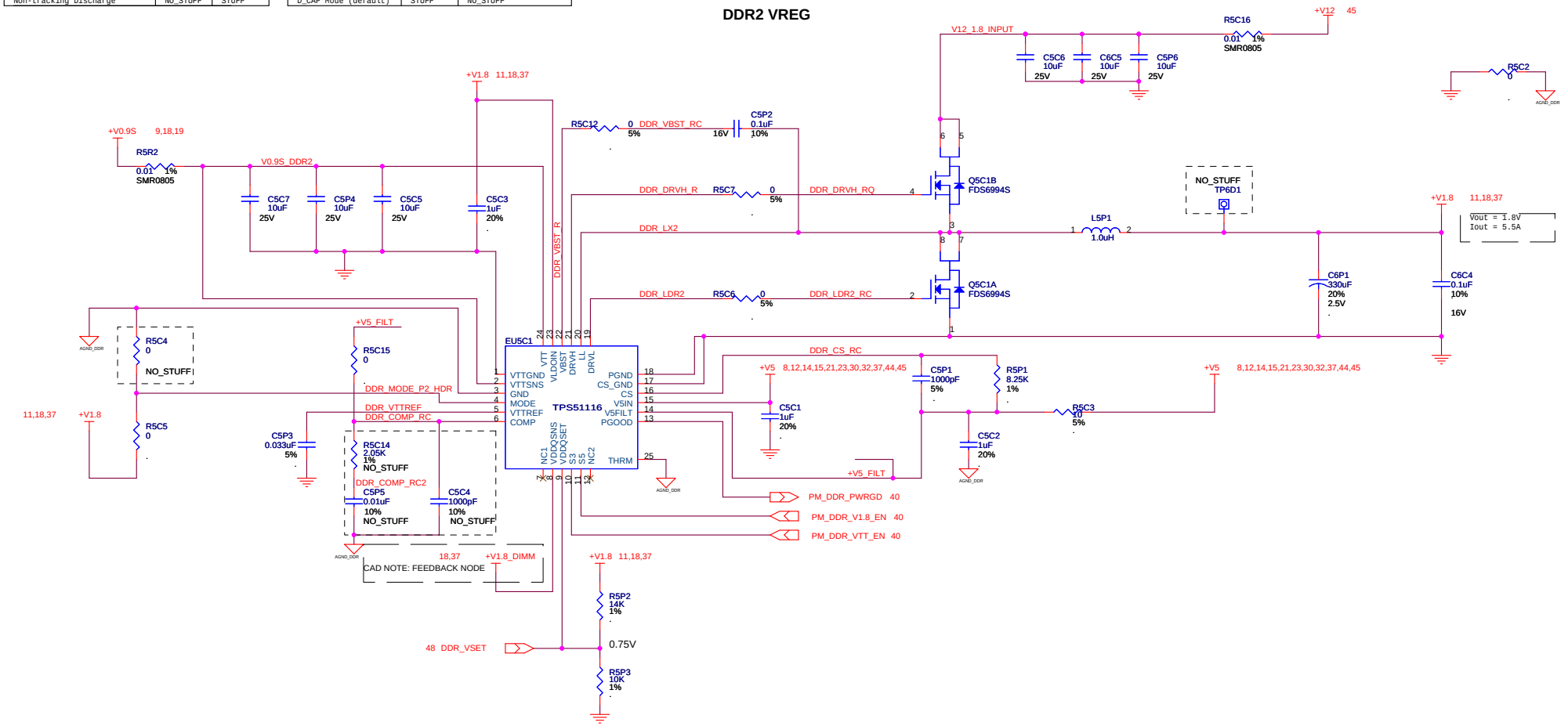
Discharge Selection		
	R5C5	R5C4
Tracking Discharge (Default)	STUFF	NO_STUFF
Non-tracking Discharge	NO_STUFF	STUFF

Mode Selection		
	R5C15	R5C14, C5P5 & C5C5
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

DDR2 VREG



Crown Beach		Intel Confidential
Title: DDR2 VR		
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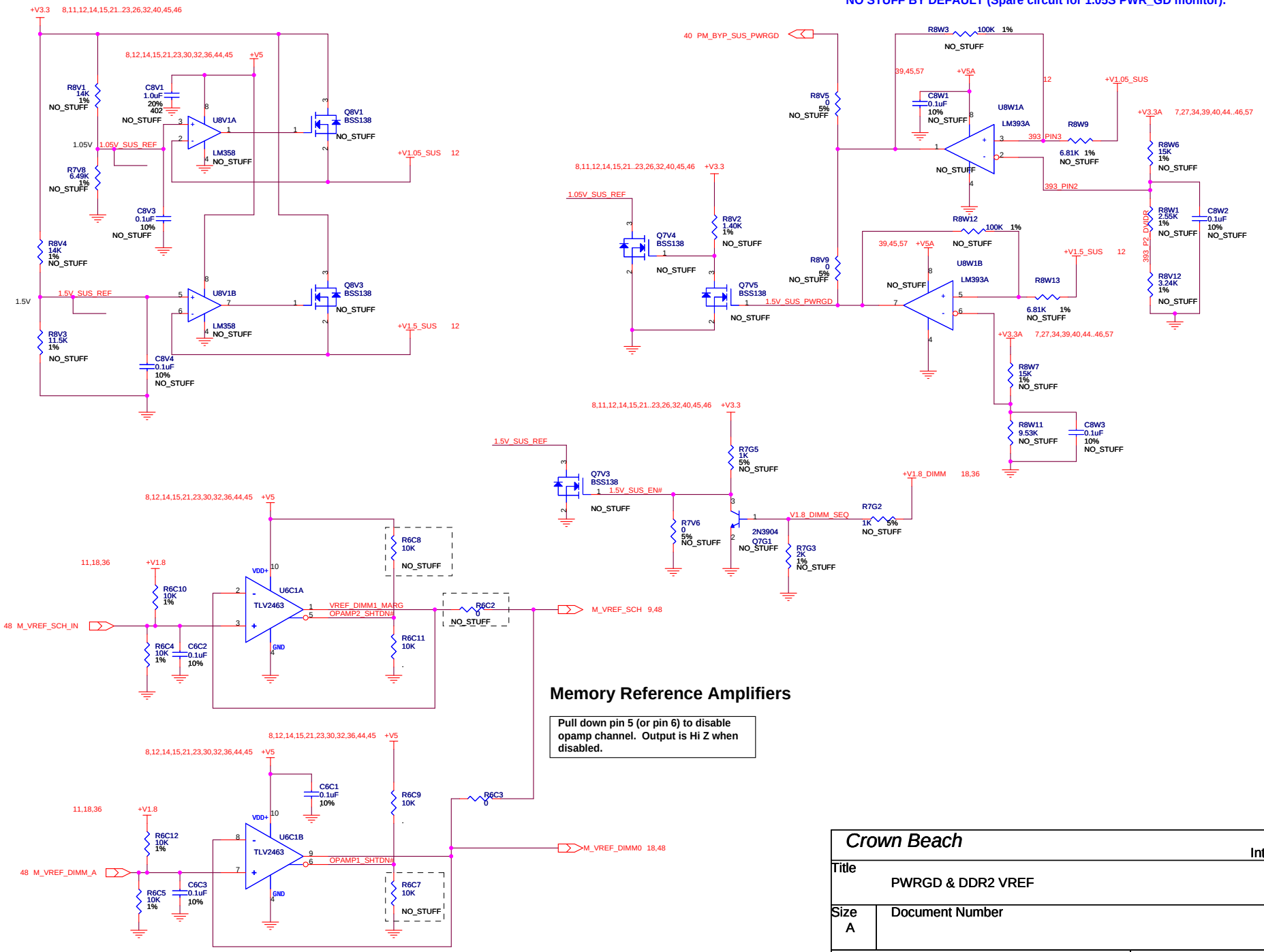
NO STUFF BY DEFAULT (Spare circuit).

NO STUFF BY DEFAULT (Spare circuit for 1.05S PWR_GD monitor).



Memory Reference Amplifiers

Pull down pin 5 (or pin 6) to disable opamp channel. Output is Hi Z when disabled.

Crown Beach		Intel Confidential
Title: PWRGD & DDR2 VREF		
Size: A	Document Number	Rev: 1.5
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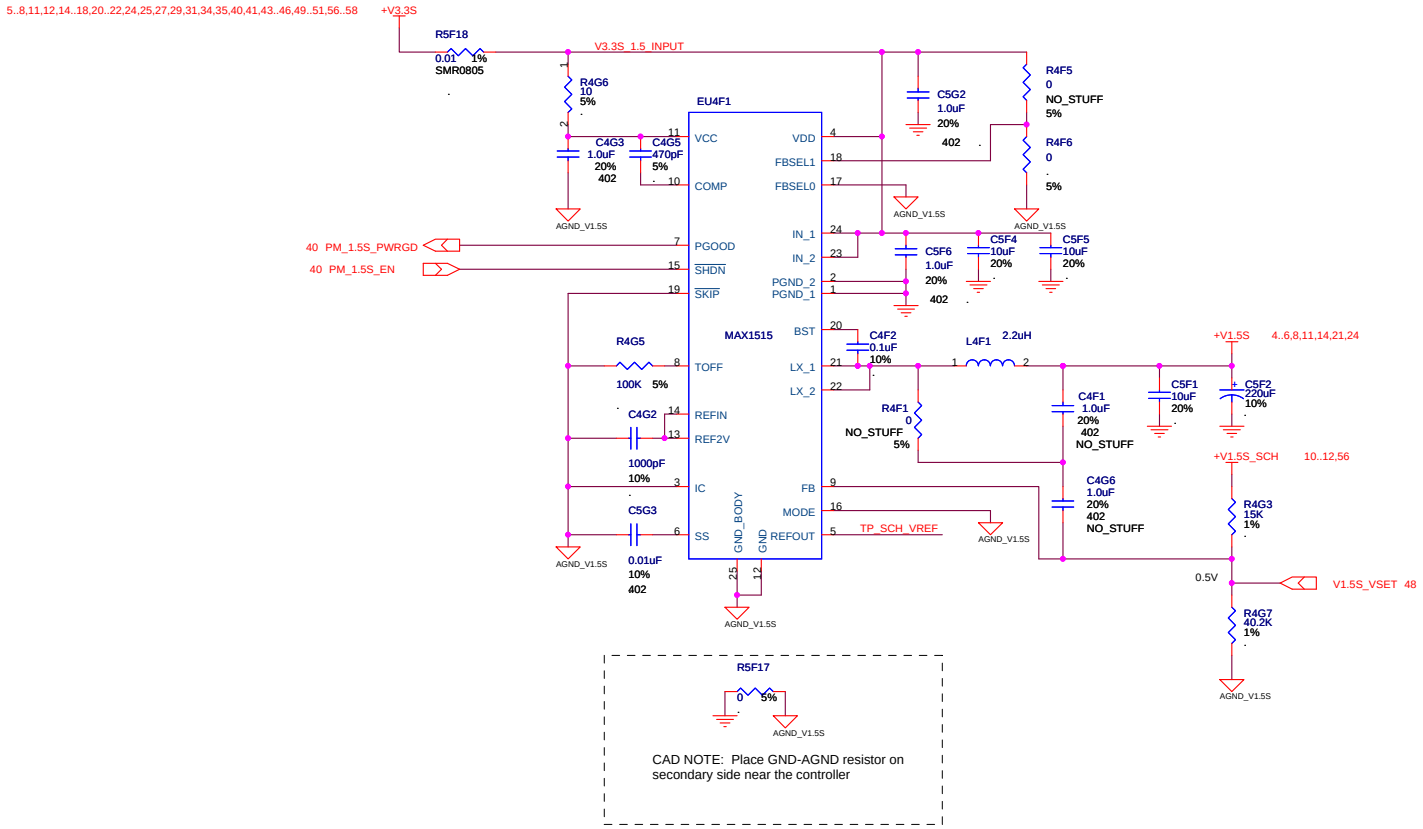

Crown Beach		Intel Confidential
Title: 1.5V VR		
Size: A	Document Number	Rev: 1.5
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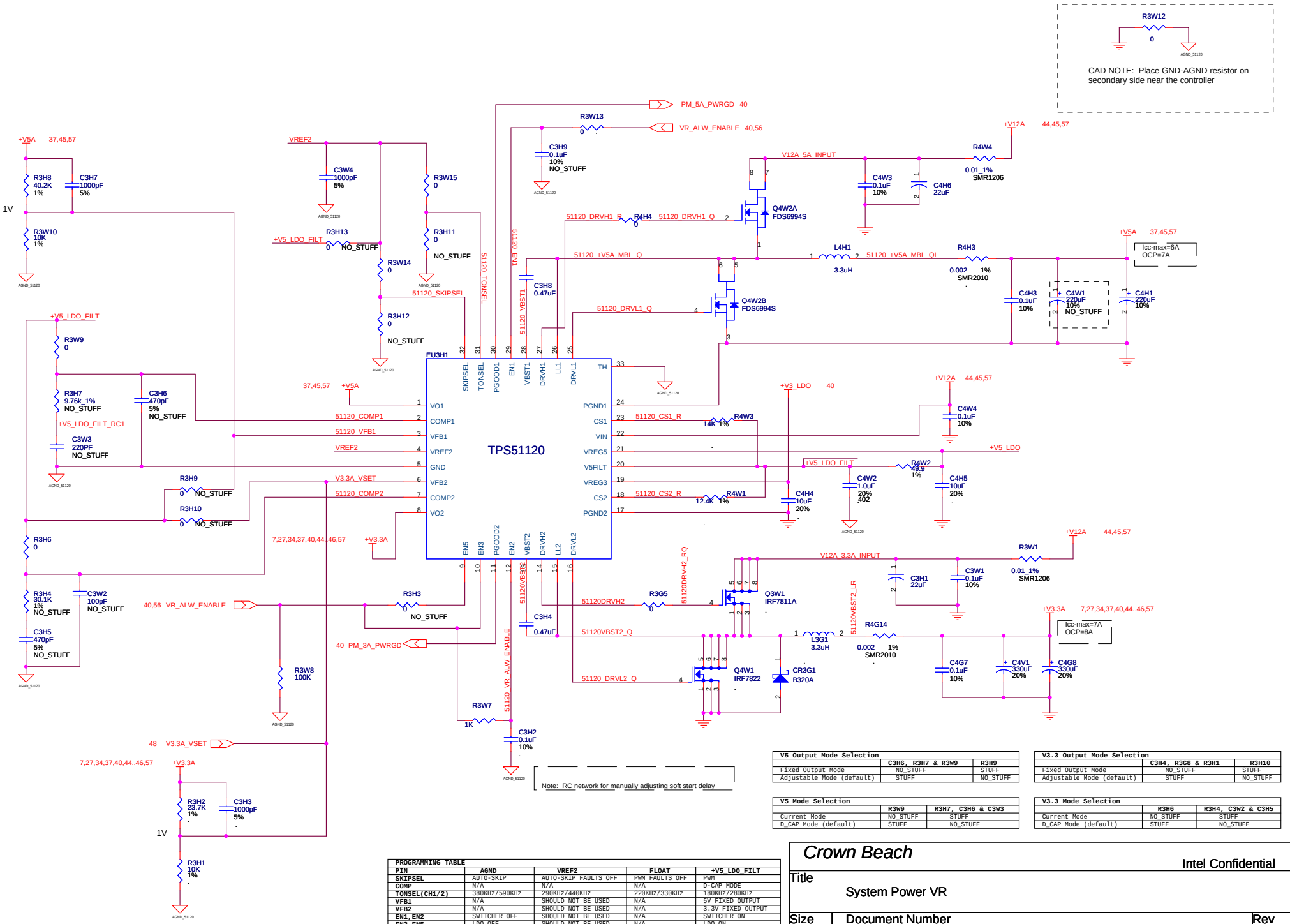

PROGRAMMING TABLE				
PIN	AGND	VREF2	FLOAT	+V5_LDO_FILT
SKIPSEL	AUTO-SKIP	AUTO-SKIP FAULTS OFF	PWM FAULTS OFF	PWM
COMP	N/A	N/A	N/A	D-CAP MODE
TONSEL(CH1/2)	380KHz/590KHz	290KHz/440KHz	220KHz/330KHz	180KHz/280KHz
VFB1	N/A	SHOULD NOT BE USED	N/A	5V FIXED OUTPUT
VFB2	N/A	SHOULD NOT BE USED	N/A	3.3V FIXED OUTPUT
EN1,EN2	SWITCHER OFF	SHOULD NOT BE USED	N/A	SWITCHER ON
EN3,EN5	LDO OFF	SHOULD NOT BE USED	N/A	LDO ON

V5 Output Mode Selection		
	C3H6, R3H7 & R3W9	R3H9
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V3.3 Output Mode Selection		
	C3H4, R3G8 & R3H1	R3H10
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V5 Mode Selection		
	R3W9	R3H7, C3H6 & C3W3
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

V3.3 Mode Selection		
	R3H6	R3H4, C3W2 & C3H5
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

Crown Beach

Intel Confidential

Title: System Power VR

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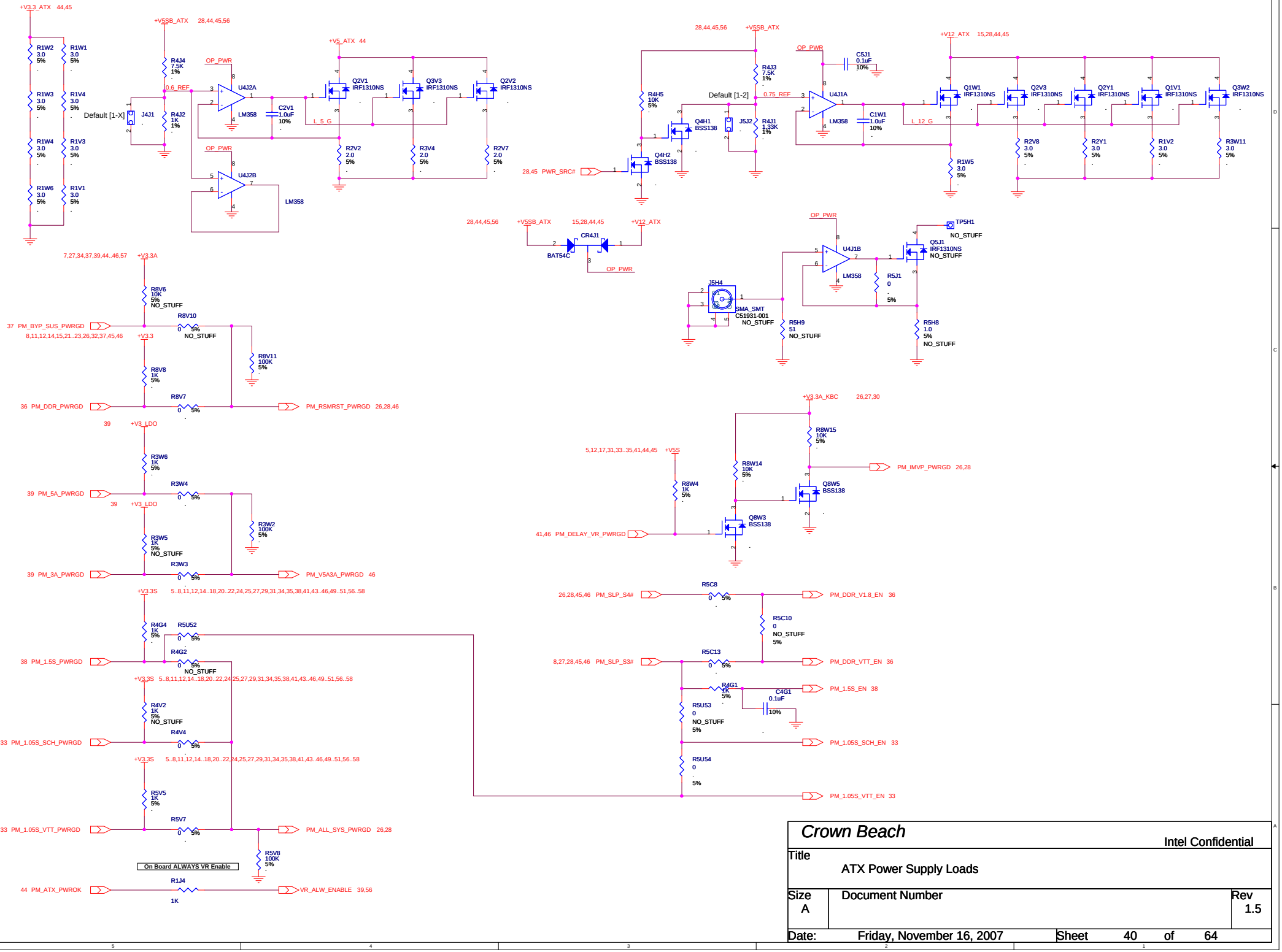

Crown Beach		Intel Confidential
Title: ATX Power Supply Loads		
Size: A	Document Number	Rev: 1.5
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IMVP-6 CORE VR

Input	Output	S2	S1	S0
A	C	1	1	0
B	C	1	1	1
~~A~~	~~D~~	1	1	1
~~B~~	~~D~~	1	1	0

Temperature Monitor

LAYOUT NOTE: PLACE Q2D1 AS CLOSE TO PHASE FET AS POSSIBLE

Q2D1 MAX6501 — GND1, GND2, HYST, TOVER#, VCC — H_PROCHOT# 3,8,48,50

+V5S 5,12,17,31,33..35,40,44,45

C2D1 2.2uF 10%

C2D2 0.1uF 10% <NO_STUFF>

+V3.3S 5..8,11,12,14..18,20..22,24,25,27,29,31,34,35,38,40,43..46,49..51,56..58

R1P10 100K, R1P8 100K, R1P7 100K, R1P5 100K, R1P4 100K, R1P2 100K, R1P1 100K, R1N3 100K

50 IMVP-4STRAP_VID0
50 IMVP-4STRAP_VID1
50 IMVP-4STRAP_VID2
50 IMVP-4STRAP_VID3
50 IMVP-4STRAP_VID4
50 IMVP-4STRAP_VID5
50 IMVP-4STRAP_VID6

J1B1 — 2X8_HDR

R1P17 1K 5%
R1P32 1K 5%
R1P33 1K 5%
R1P34 1K 5%
R1P35 1K 5%
R1P36 1K 5%
R1P37 1K 5%
R1P38 1K 5%

J1B1 DEFAULT SHUNTS:
[1-2], [3-4], [5-6], [7-8], [9-10], [11-12], [13-14]

J1B1 [15-16] :
Shorted for manual VID operation
No Jumper for CPU driven VID operation (Default)

U1C1 — 74CBT16209A

4,5 H_VID0
4,5 H_VID1
4,5 H_VID2
4,5 H_VID3
4,5 H_VID4
4,5 H_VID5
4,5 H_VID6

VR_VID0, VR_VID1, VR_VID2, VR_VID3, VR_VID4, VR_VID5, VR_VID6

50 V3_S0

V3_S0, S2_S1

R1P6 10K 5%

+V5S 5,12,17,31,33..35,40,44,45

C1P1 .01uF

+V5S 5,12,17,31,33..35,40,44,45

R3C9 0.01 1% SMR0805

42 V12_CPU_PHASE

R2C2 10 1%

8770_VCC

V5S_IMVP_IN

C2C2 2.2uF 10%

C2C1 2.2uF 10%

C3C3 22uF 20% SMC0805

R2B6 140K 1%

4,5,42,43 +VCC_CORE

EU2B1

Intel(R) VMP-6 Controller

R2B7 71.5K 1%

C3B9 470pF 5% NO_STUFF

C3B10 1500pF 10%

C3B8 0.22uF 10%

8770_OSC
8770_TIME
8770_CCV
8770_CCI
8770_REF

8770_BST1 42
8770_DH1 42
8770_LX1 42
8770_DL1 42

CSP1 42
LX1_FBK 4,42

TP_8770_DH2
TP_8770_LX2
TP_8770_DL2
TP_8770_BST2
8770_CSP2
VCC_SNS_R

40,46 PM_DELAY_VR_PWRGD
34 VR_VID0
34 VR_VID1
34 VR_VID2
34 VR_VID3
34 VR_VID4
34 VR_VID5
34 VR_VID6

26,28 IMVP_VR_ON
7,21 PM_DPRSLPVR

J2B1
3 PSI#
3,6,21,50 H_DPRSTP#
CPU_PWR
24 VR_PWRGD_CLKEN#

8770_VRHOT#

R2B10 2.2K
R2B8 10K

5..8,11,12,14..18,20..22,24,25,27,29,31,34,35,38,40,43..46,49..51,56..58 +V3.3S

8770_THRM

8770_GNDS

+V5S 5,12,17,31,33..35,40,44,45

R3C8 0 5%

8770_FB

C3B12 1000pF 10% NO_STUFF

R3B9 7.5K 1% NO_STUFF

R3B8 3.74K 1%

C3N2 1000pF 10%

R2N7 8.25K 1%

8770_VCC

C2N5 1000pF 10%

RT2N1 100K

+V5S 5,12,17,31,33..35,40,44,45

R3C11 0 5%

J3C2

CON3_HDR NO_STUFF

R3C10 100K 5%

INTER# 1

Q3C1 BSS138 NO_STUFF

C3B11 1000pF 10%

R3B10 0

Place R3B10 close to GND (Pin 18)

Route to Die Sense Pins as Differential Pair.

R3N4 10 1%

R3P1 10 1%

VSSSENSE 4

VCCSENSE 4

R3C1 27.4 1% NO_STUFF

J3C1

R3C2 27.4 1% NO_STUFF

Place near controller

Layout Note: use 27.4 Ohm routing for Vssense and Vccsense

Crown Beach		Intel Confidential
Title: IMVP-6 Controller		
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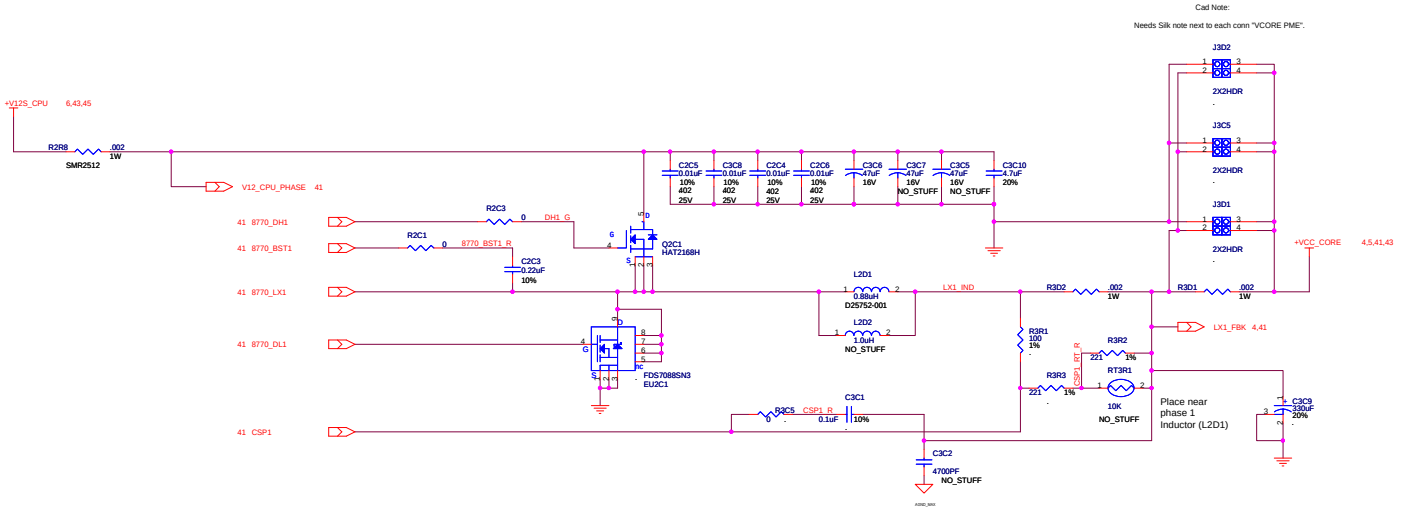

Crown Beach		Intel Confidential
Title: IMVP-6 Core VR Phases		
Size: A	Document Number	Rev: 1.5
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Vcc Core Decoupling

4,5,41,42 +VCC_CORE

Isolation resistor on the VR page

16 x 1uF (A36096-044) 0402
Place CPU Die Shadow - Secondary side

C3T20 C3T26 C3T28 C3T22 C3T31 C3T36 C3T40 C3T38 C3T21 C3T18 C3T41 C3T30 C3T42 C3T32 C3T27 C3T37
1.0uF 20% 402

14 x 10uF (602433-075) 0603
Need to identify specific parts to meet ESR/ESL
Place between VR and CPU plane

C3T3 C3T11 C3T5 C3T6 C3T4 C3T2 C3T7 C3T15 C3T12 C3T8 C3T9 C3T10 C3T14 C3T13
10uF 0603 20% <VOLTAGE> CPU

Place around the CPU socket

Three 330uF (C71589-001) Secondary Side

C3D1 330uF 20%
C3R1 330uF 20%
Takasago Low ESL Capacitors

3,4,11,29,33,48,50 +V1.05S_VTT_CPU +VCCP1.05_CPU_C6_OFF 3,4

6,42,45 +V12S_CPU

C1E4 330uF 20% 2.5V

R2F11 100K 1%
R2F3
R2F2 0 5%
Q2F1 IRF6623
Q2F3 IRF5851
Q2F2 IRLML2402
R2F5 100K 1%
C2F1 0.1uF 10%

5..8,11,12,14..18,20..22,24,25,27,29,31,34,35,38,40,41,44..46,49..51,56..58 +V3.3S

R2F1 0 5% NO_STUFF
J2F1 CON3_HDR
8,29 SLPIOVR#

Default [1-2]
Split Vtt Control
1-2 = GPIO controlled
2-3 = Force VCCP OFF
Open = Force VCCP ON

R2F4 1K 5%

SLPIOVR# = 0(C6) => Switch OFF +VCCP1.05_CPU_C6_OFF = 0
SLPIOVR# = 1(Normal) => Switch ON +VCCP1.05_CPU_C6_OFF = +V1.05S_VTT_CPU

12 x 1uF (A36096-044) 0402
Place CPU Die Shadow - Secondary side

C3T48 C3T52 C3T29 C3T47 C3T55 C3T39 C3T49 C3T35 C3T50 C3T53 C3T45 C3T25
1.0uF 20% 402
NO_STUFF

8 x 0.1uF (A36096-043) 0402
Place CPU Die Shadow - Secondary side

C3T43 C3T33 C3T23 C3T34 C3T44 C3T46 C3T24 C3T54
0.1uF 10% SMC0402
NO_STUFF

Crown Beach		Intel Confidential
Title: CPU Decoupling		
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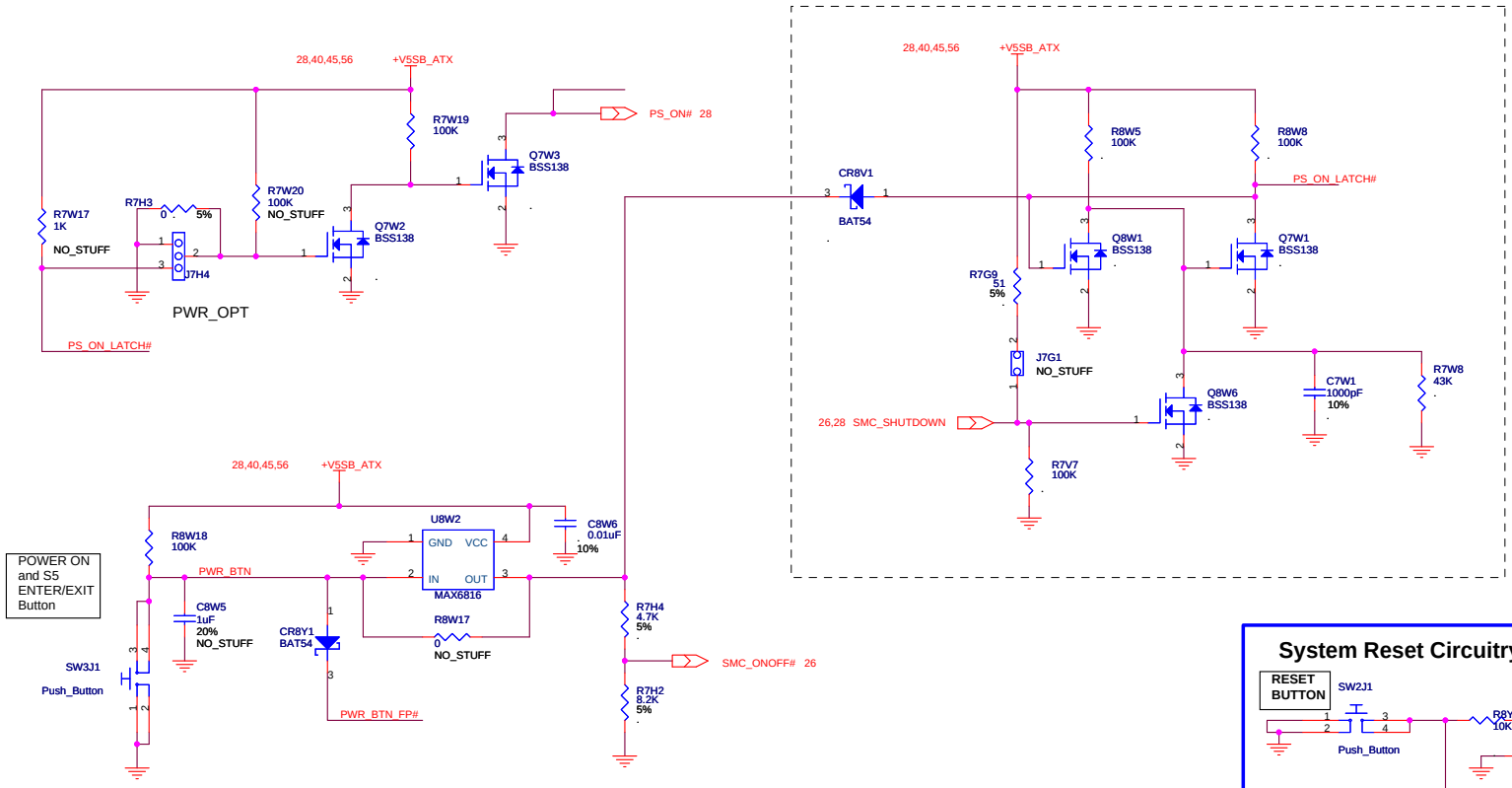
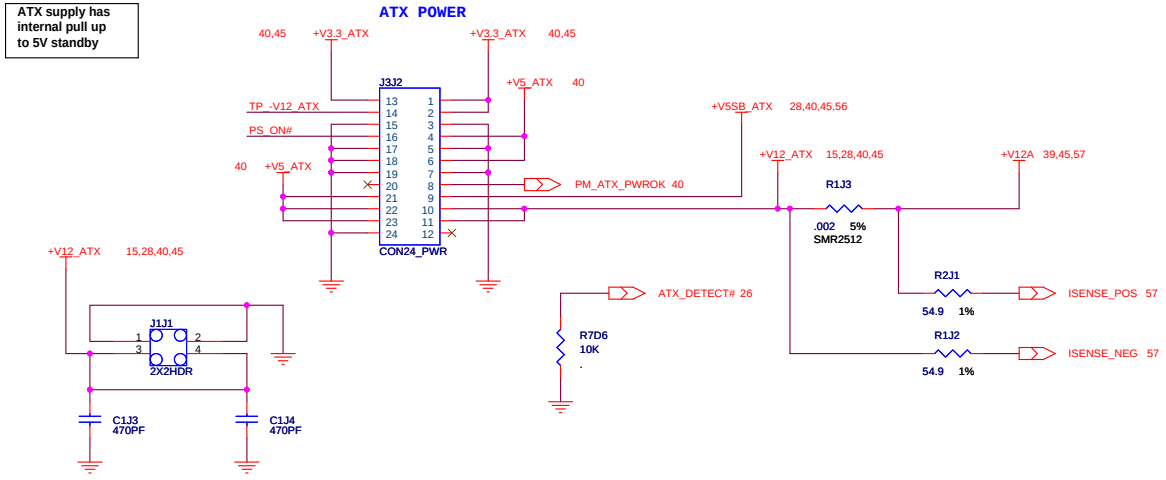
Switch Control and On Board VR Enable Circuitry

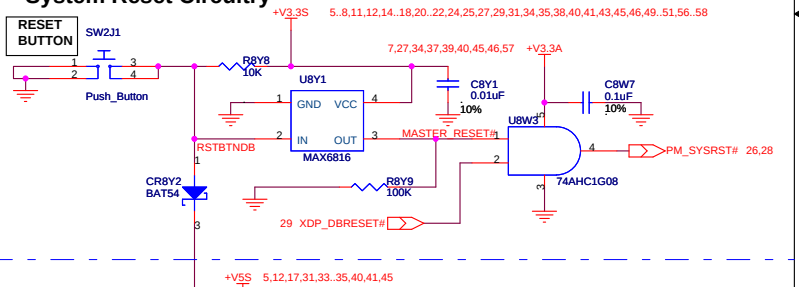
(see Notes for signal description)



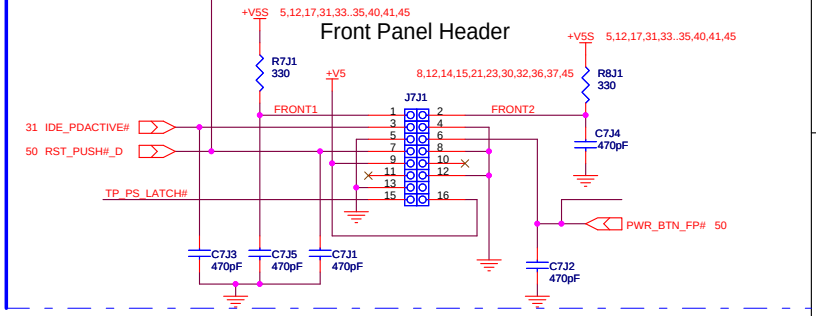
ATX POWER



System Reset Circuitry



Front Panel Header



Crown Beach		Intel Confidential
Title: Start Up Sequence		
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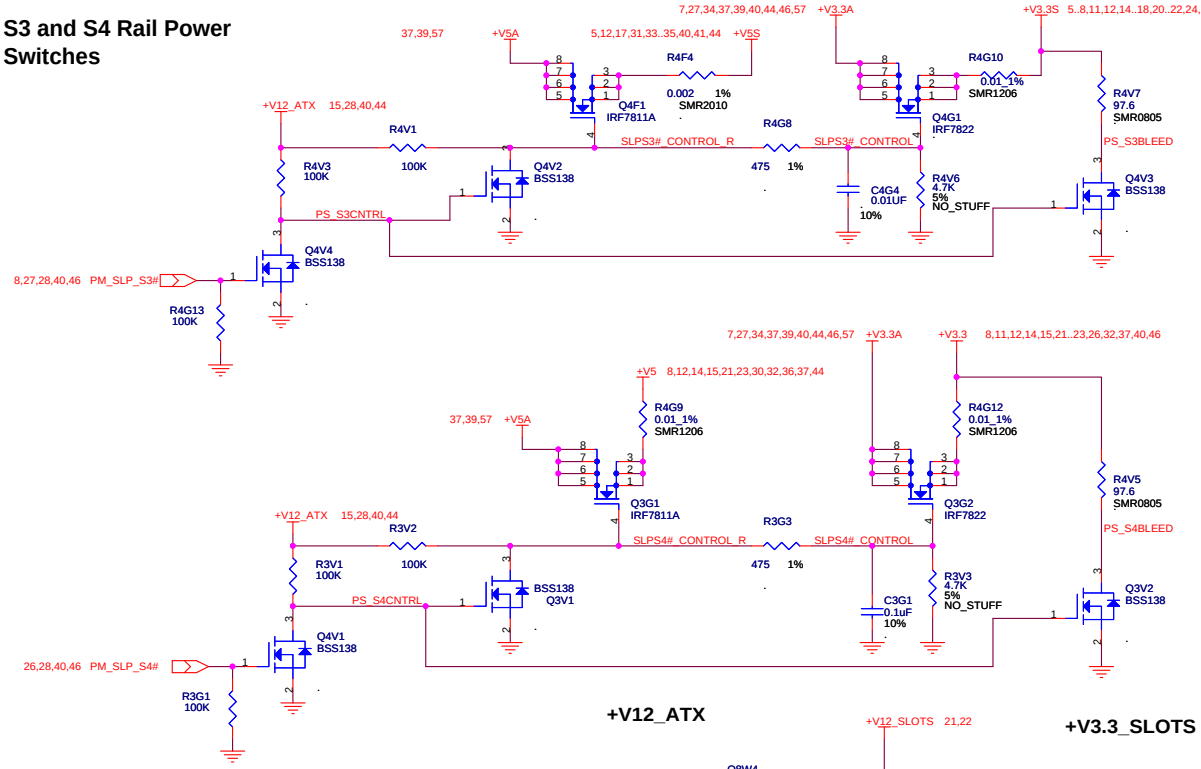
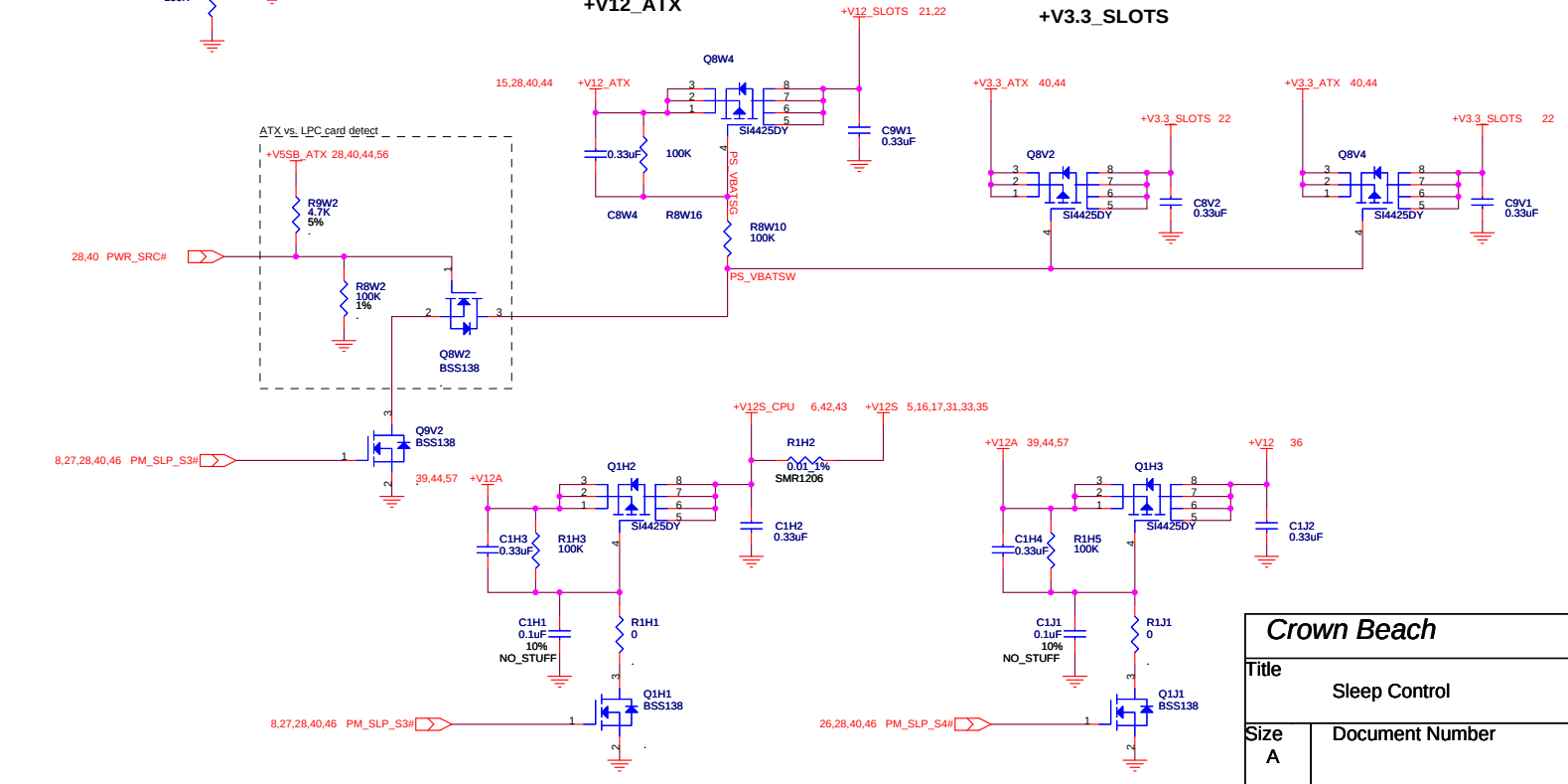
S3 and S4 Rail Power Switches



+V12_ATX



+V3.3_SLOTS

Crown Beach		Intel Confidential
Title: Sleep Control		
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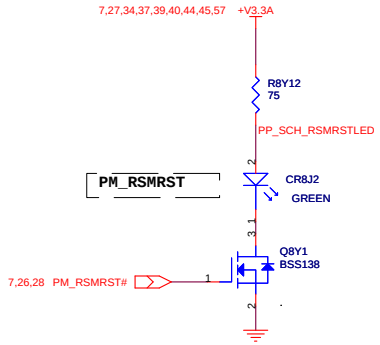
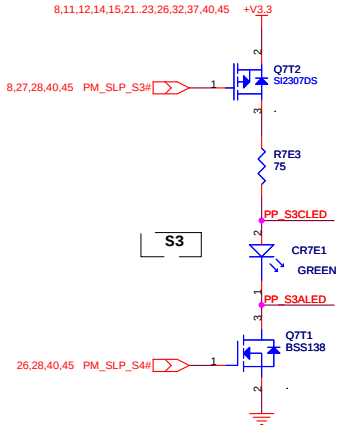
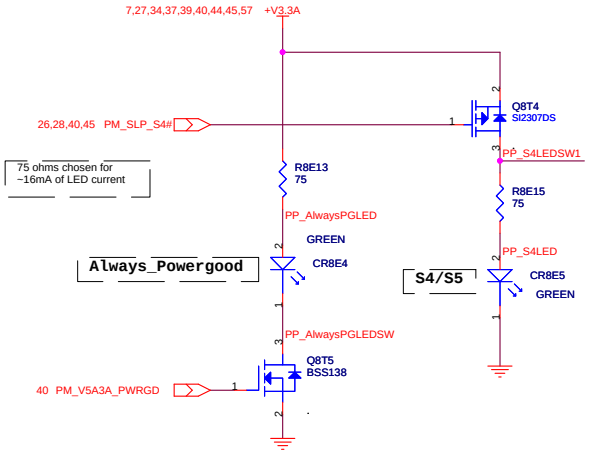
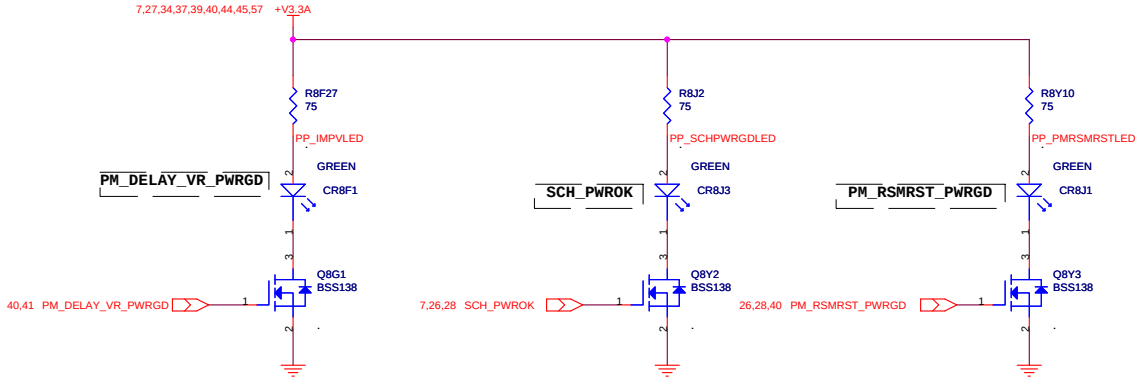
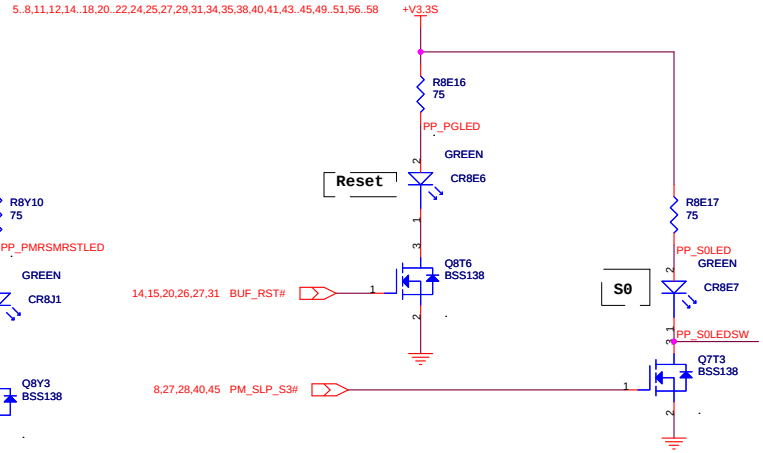
SYSTEM STATE LEDS

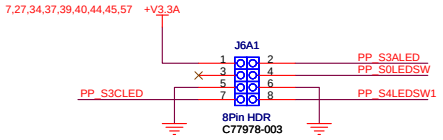


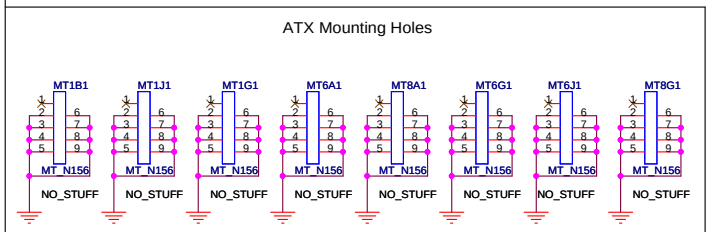












Crown Beach		Intel Confidential
Title: ATX Mounting Holes - LEDs		
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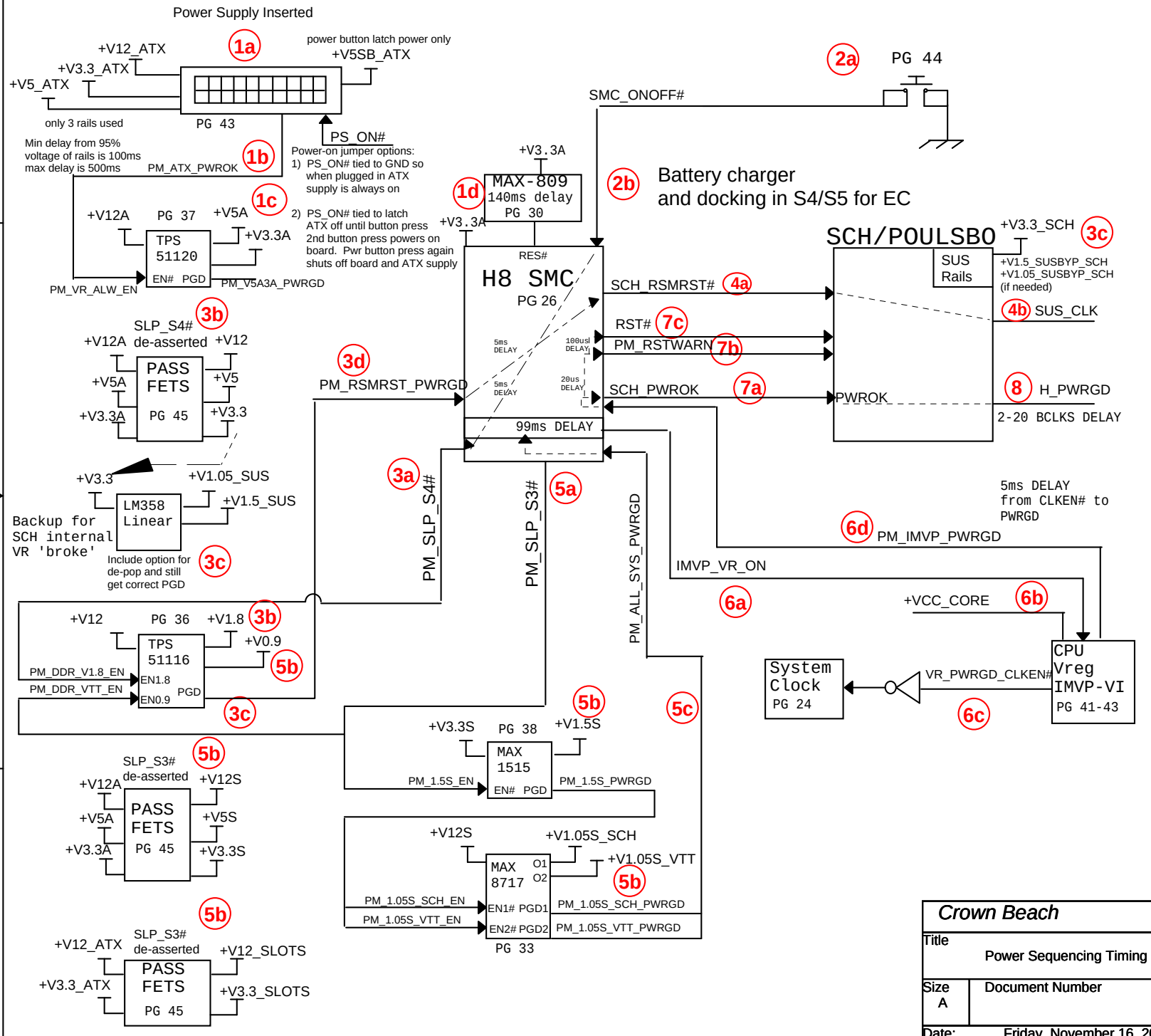
CROWN BEACH VV/CEB Power On Sequence v0.9



1) ATX supply plugged in (a). ATX PS_ON# clamped low for always "on". PM_ATX_PWROK asserted once the power rails are stable (b). PM_ATX_PWROK is enable for the TPS51120 to begin regulation of +V5A & +V3.3A (c). The H8 has it's own power good indicator from MAX809 (d).

2) Power Button pressed (a) which momentarily asserts SMC_ONOFF# (b).

3) H8 de-asserts PM_SLP_S4# (a) +V5 & +V3.3 pass (b) +V3.3 is used to generate +v1.05SUS and +V1.5SUS if the SCH internal VReg is broken and +V1.8 begins regulation (c). PM_RSMRST_PWRGD signifies that the 1.8V rail is "good".

4) H8 de-asserts SCH_RSMRST# after receiving PM_RSMRST_PWRGD (a). SCH begins driving SUS_CLK (b).

5) H8 de-asserts PM_SLP_S3# (a). +V0.9, +V5S, +V3.3S go active as well as +V12_SLOTS and +V3.3_SLOTS ; +V1.5S, +V1.05 (SCH & VTT) go active (b). PM_ALL_SYS_PWRGD is asserted to the SCH (c).

6) H8 asserts IMVP_VR_ON (a). Controller ramps to the 1.20V boot voltage (b). Controller asserts VR_PWRGD_CLKEN# ~60usec later (c). Controller releases PM_IMVP_PWRGD (from holding it low) 5msec later (d).

7) SCH_PWROK is asserted (a). H8 waits at least 20usec before asserting PM_RSTWARN to SCH (b) and then another 100usec from PM_RSTWARN assertion before asserting RST# to the SCH (c).

8) SCH asserts H_PWRGD to the CPU.

Crown Beach		Intel Confidential
Title: Power Sequencing Timing Block Diagram		
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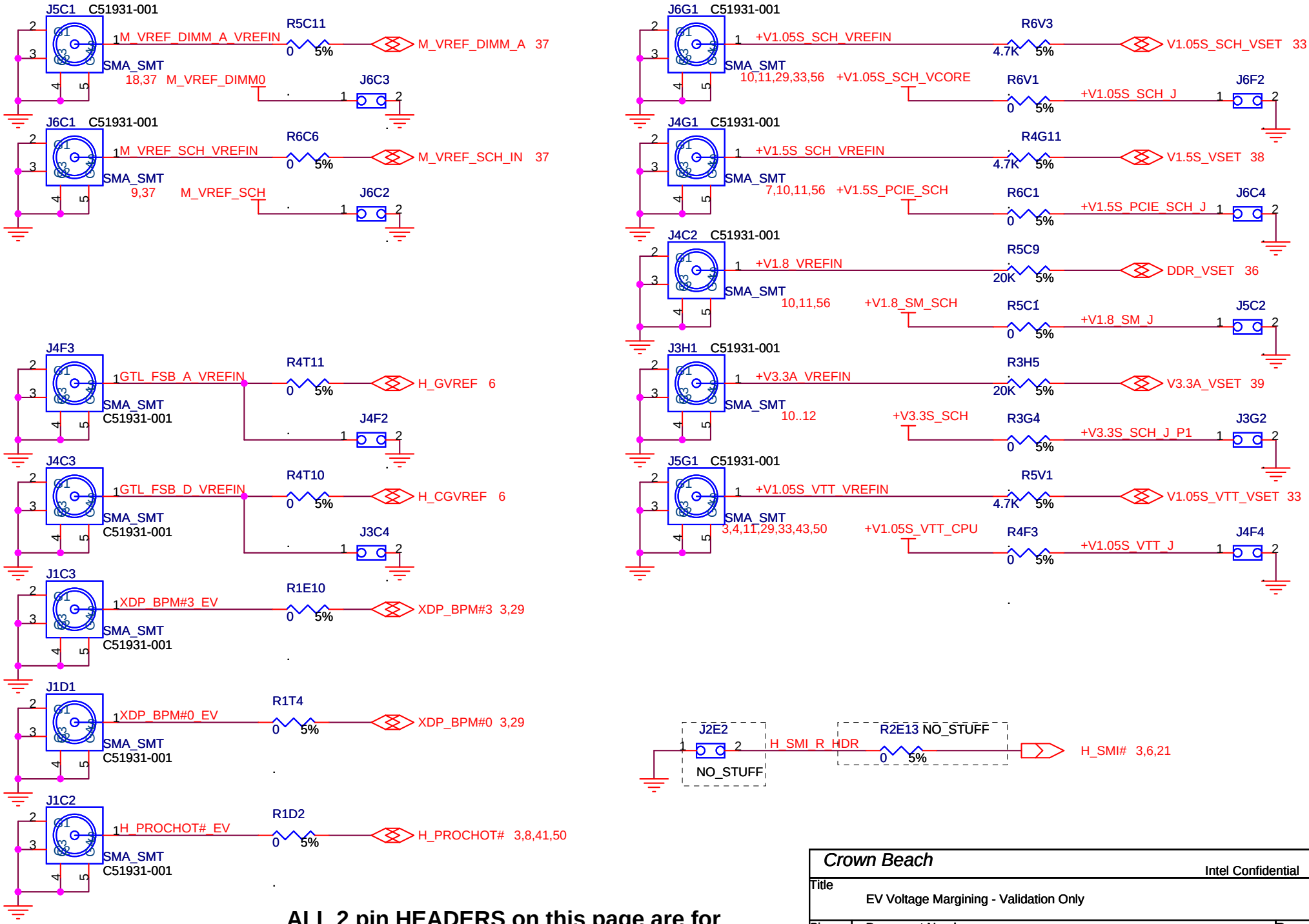

ALL 2 pin HEADERS on this page are for measurement only, do not shunt

Crown Beach		Intel Confidential
Title: EV Voltage Margining - Validation Only		
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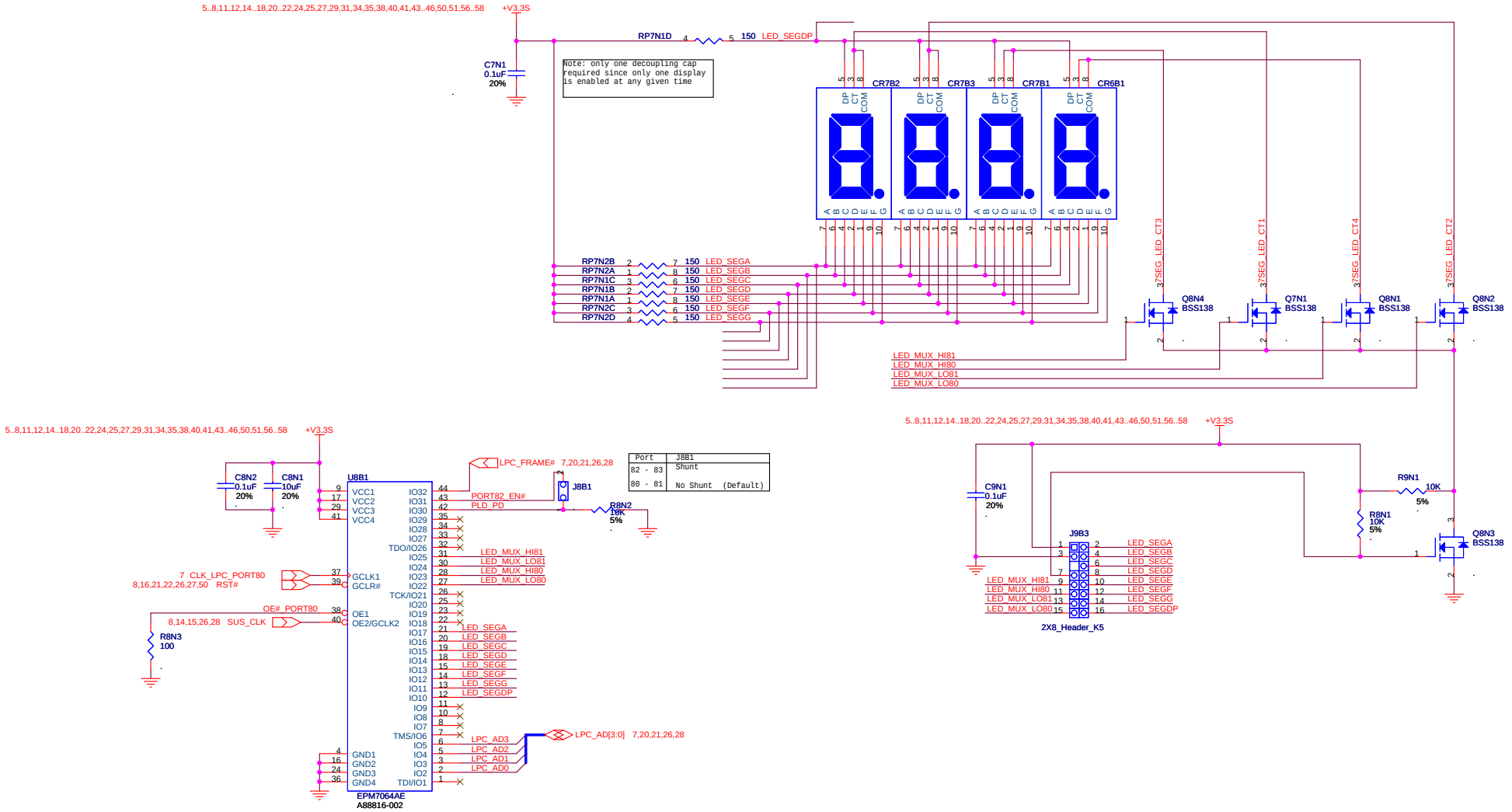
PORT 80-83 DISPLAY

High Nibble (CR7B2) Port 80/82 High Nibble (CR7B1) Port 81/83
Low Nibble (CR7B3) Port 80/82 Low Nibble (CR6B1) Port 81/83



Crown Beach			Intel Confidential
Title: Port 80-83 - Validation Only			
Size: A	Document Number:		Rev: 1.5
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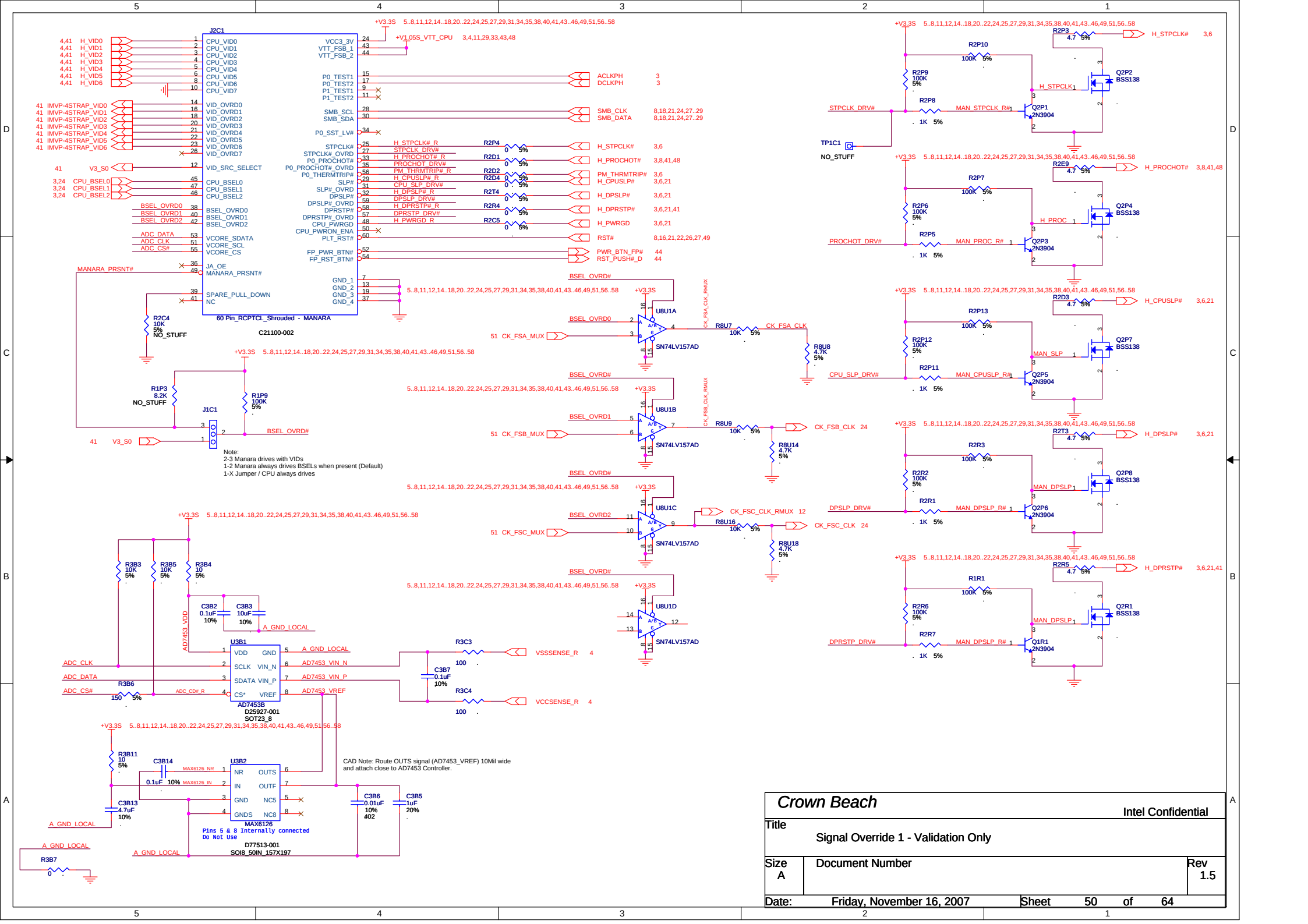
J2C1
60 Pin_RCPTCL_Shrouded - MANARA
C21100-002
Note:
2-3 Manara drives with VIDs
1-2 Manara always drives BSELs when present (Default)
1-X Jumper / CPU always drives
U3B1
AD7453B
D25927-001
SOT23_8
U3B2
MAX6126
Pins 5 & 8 Internally connected
Do Not Use
D77513-001
SOI8_50IN_157X197
CAD Note: Route OUTS signal (AD7453_VREF) 10Mil wide and attach close to AD7453 Controller.
U8U1A
U8U1B
U8U1C
U8U1D
SN74LV157AD
Crown Beach
Intel Confidential
Title
Signal Override 1 - Validation Only
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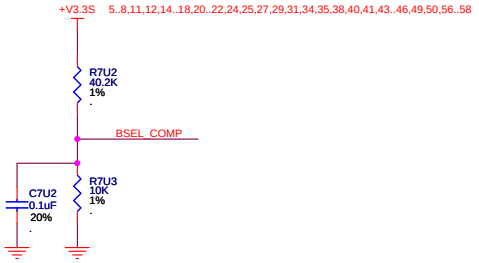
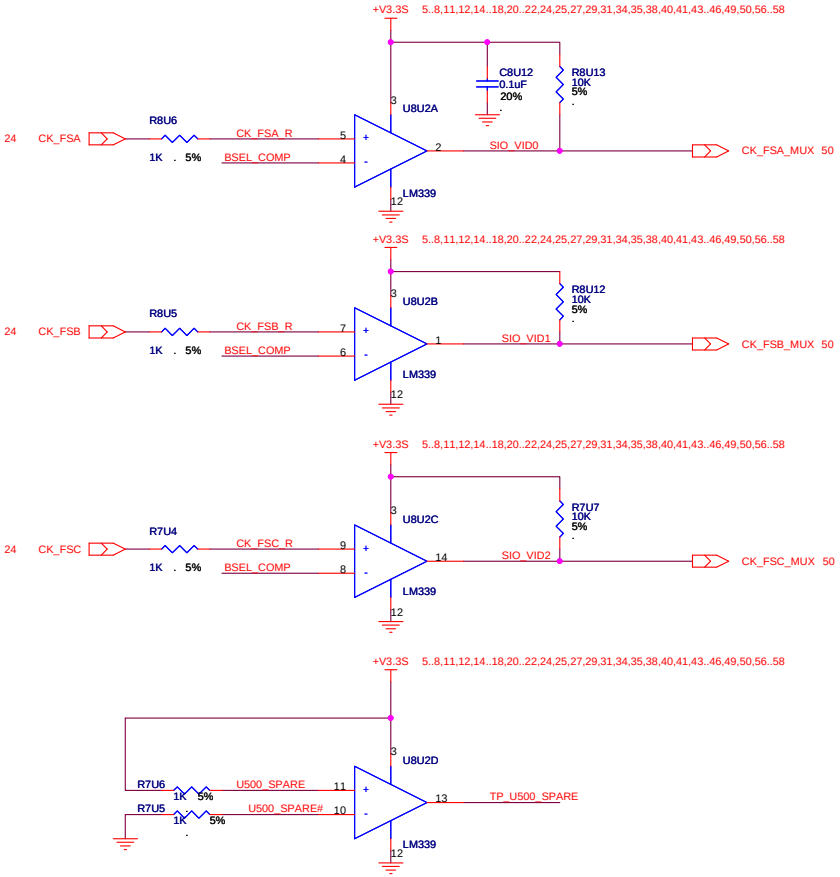
BSEL COMPARATOR REFERENCE





Crown Beach		Intel Confidential
Title: Signal Override 2 - Validation Only		
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Rev 0.5 External

Initial Release

Rev 1.0 External

Added PWRGD switching circuit.
Emptied C1H1 and C1J1.
Changed R1H1 and R1J1 from 100K to 0 ohm.
Added stuffing option on SDIO 1 bits 5-7.
More stuffing on SDIO PWR.
H8 connections for above SDIO options.
Added 10K pd on IDE_PDDREQ.
Added 0.047uF in parallel with R6J4 and emptied R.
Inserted new pg for second PCIe MINI Card.
Add 10 up to INT_SERIRQ.
R7, R8, and R9 changed to 1K Stuffed.
Updated H8 bypass conn model to pull out two gnds and change to TX and RX pins.
Added 0 ohm series to KBC_PROG_XX# and changed net SMC_ONOFF# to PS_ON#.
Added CMOS_EN FET switch to CPU_CMREF.
Added CMOS_EN circuit to H_CGVREF.
Changed R9D2 to 1K.
Reversed TX and RX on minicard conns.
Reconnected pins 37, 39, 41 and 43 per new spec.
Pins 2 and 52 now connect to 3.3Aux, moved decoupling to that rail.
Removed SLOT2_CLK_MINI and SLOT2CMD_MINI nets from conn and renamed net to isolate from minicardA.
Changed Q8U2 to BSS138.
Emptied C8U8 and C9U7.
Added three pu's on the SLOTx_CD nets on the Poulsbo side of the option resistor.
Changed H8S/2104 BGA to H8S/2117 PQFP.
Added 0ohm option on RSVD13-17 for USIM.
Added Pink and Green jacks, 4 3-pin hears for power options on conn. Deleted two LEDs.
Added RS232 tranceiver and bypass option.
Added stuffing option on miniPCIe for SMBus (pins 30&32).
Added stuffing option for 1.5v on pin 28 for STD miniPCIe.
Change C7V11 to 10uF.
Add a series 0ohm resistor to pin 22 of J7H4.
Add THM test points on SLOT0_CD#, SLOT0_WP, SLOT0_LED.
Empty R5B1(R5B5), R5B2(R5B6), R5N3, R5N2, R7, R8, and R9.
Empty R10, R11, R12.
Add series 1k res to pin 1 of Q9D2 (INIT# FET) and change FET Q9D2 to MMBT3904 (NPN).
Add three stuffed 0 ohm resistors connected between SD0PWR# and SLOT1-DATA5; SD1PWR# and SLOT1_DATA6; SD2PWR# and SLOT1_DATA7.
CAD note please place these resistors near J5B1.
Empty R5U8, R5F4, R5F7, stuff R4, R5, R6 with 221ohm 0402.
Empty J9G3 and remove from table.
Unstuffed R13.
Added back in the two audio jacks.
Added new net WWAN_nINTR to pin 44 of conn.
Connection made for above new net to pin 58.
Added 1K pd on PSI.

BOM updates:
R6T22, R5U36, R5U1
Empty C5T1
Empty R5H5
Emptying COMMs added parts for typical boards.
Empty R8F6
Reversed stuffing son 2104 options
R5V3/R5V6 reversal.
Changed all 3.3 loads to 3 ohms.
Stuff R8Y13 and R8J3.
Empty U9D1 and Stuff R7E1.
Change R5U17 and R5U11 to 10ohms.
Stuff R5U8.
Change the following 0ohms:
R8F7, R8F9, R8F11, R8F12, R8F14, R8F16, R8F18, R8F17, R8F22, R8F20, R8F26, R8F24, R8F23, R8F25, R8F8, R8F10, R8F15, R8F13.
Updated Poulsbo to incorporate B0 changes into model.

Rev 1.5 External

Emptied TP6B1, TP6B2 and TP6B3.

Changed R2E3 from 1K to 402.
Changed R4R7 to 75K.
Changed R2F3 to 10K and stuffed C2F1 with0.1uF

Changed R5V22 and R5V27 to 470 ohm.
Emptied C6N1, C4B2 and C4B1.

Changed SMA footprints to 4 footed.
Changed nets on U9J1 10,13 to xxx_TXD.
Deleting R8U4 and Q8U1, to remove the inverter.
Swap nets PMU_4 and H8_PIN115 on U9D1
Deleted MANARA_PRSNT# net and FET and changed VID over ride pull-ups.
Added 330uF to +V1.05S_VTT_CPU.
Made MANARA_PRSNT# net local to this page only.
Moved 8.2K pu here from pg 40 and emptied.

Added 0ohm in series from +V1.05S_VTT_CPU to J2E1 pin 1.
Added empty 0 ohm from J2E1 pin 1 and +VCCP1.05_CPU_C6_OFF.
Added testpad on TP_GPIOSUS_0
Added FSC option into 3 pin header selection for BSEL0.
Added offpage on CK_FSC_CLK_RMUX

Connected GPIOSUS_0 to pin 34 on IDE
Connected GPIOSUS_0 to pin 34 via series 0 ohm.

Updated SLT model to fix naming inconsistency.
Change R5U17 and R5U11 to 22 ohm. Unstuff R5U8.
Change R1 to 100 ohm, empty R5H1 and R5H4,
Stuff R5H2 and R5H5
Empty R7E1
Empty R8J3 and R8Y13
Change R2F3 from 10K to 2K.

Changed R2V2, R3V4 and R2V7 to 2.0ohms

Stuffed U9J1, J9G6, C9J1, C9J2, C9J3, C9J4, C9J5
C9J6, R9J4, R9J5, R9H4, R9H1, R9H6, R9J1.
Emptied R8Y11, R8T11 and R7T12.
Stuffed R8R4, R8T10, R7T11, R8T12 and R8T8.
Emptied R4R3 and R4P8.
Stuffed R4R2 and R4P7.

Added four 0 ohms for stuffing option to UART.
Added four nets to complete the 232 connections.
Made connections match from UART option to H8

Changed PCIe stuffing- Emptied R6E6,
R6E7, R6D4, R6D2, R6E4 and R6E7.
Stuffed R6E5, R6E8, R6D3, R6D1, R6E3 and R6E2.
Emptied C3T49, C3T50, C3T52, C3T53, C3T54 and C3T55 for C6 adjustments.

Added four pull-ups to SLT RSVD[3:0] SLT.

Added ESD diode to client conn.

Emptied Q4C2 and stuffed R3C6 to bypass

Changed R3E13-16 from 1K to 0 Ohm

Changed jumper settings for J8G3 and J9G3 to 1-2 and made that default.

Crown Beach		Intel Confidential
Title: Revision History		
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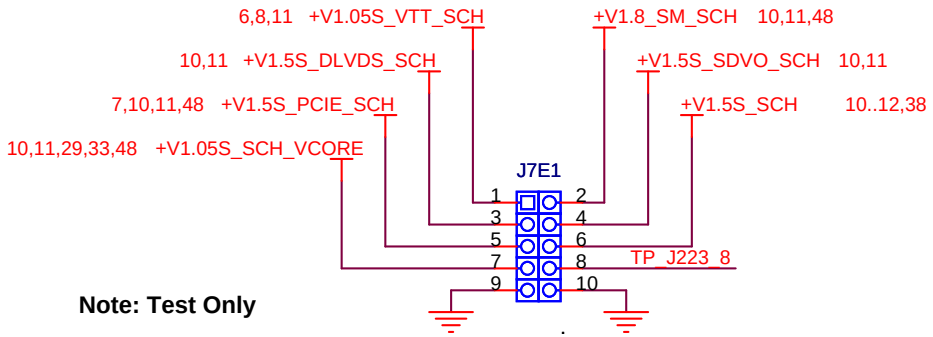
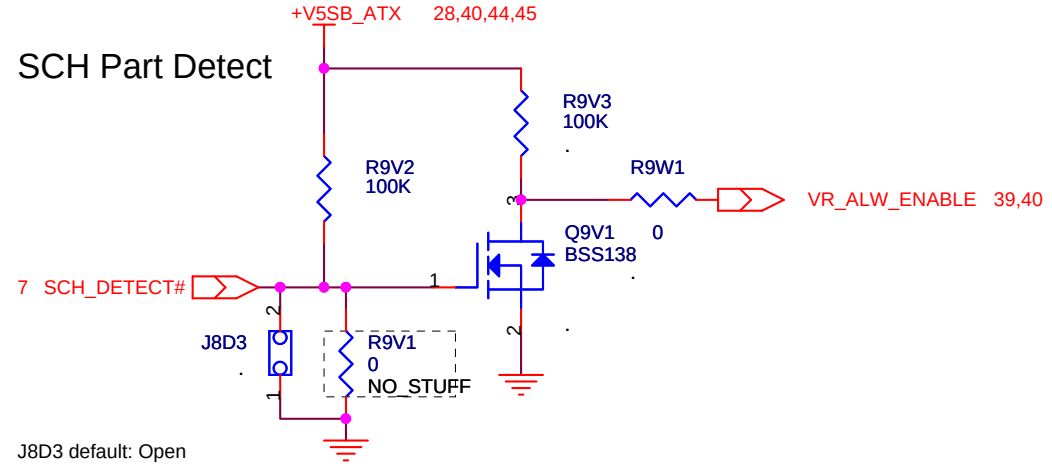
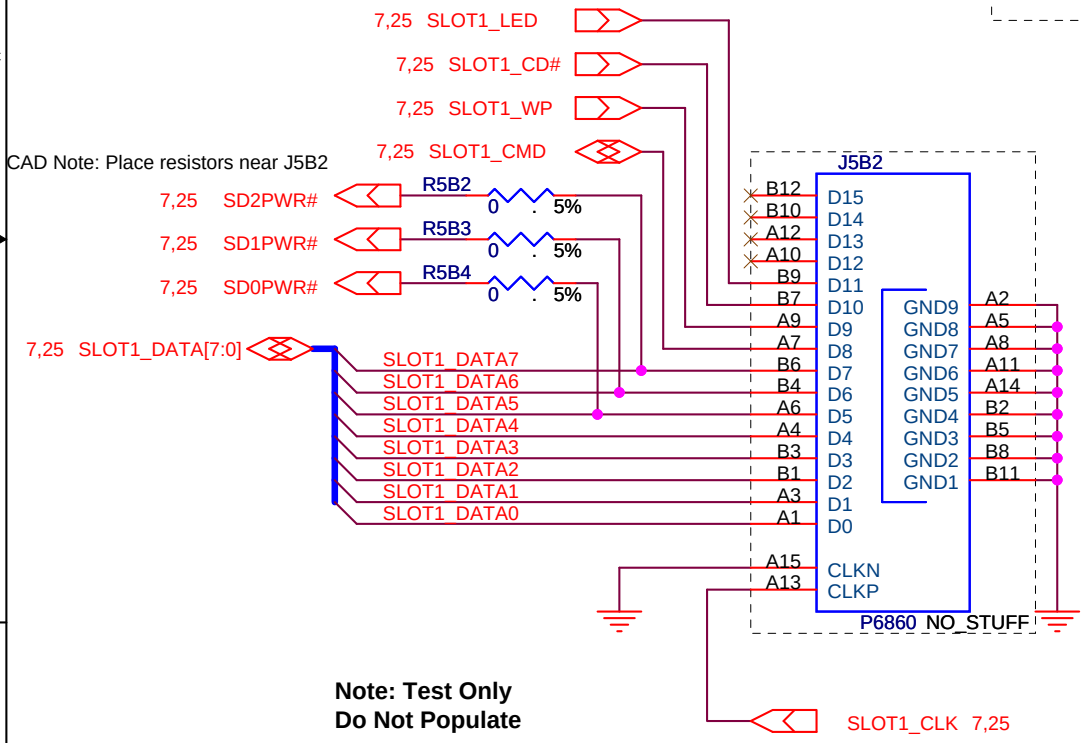


Note: Test Only

SCH Part Detect



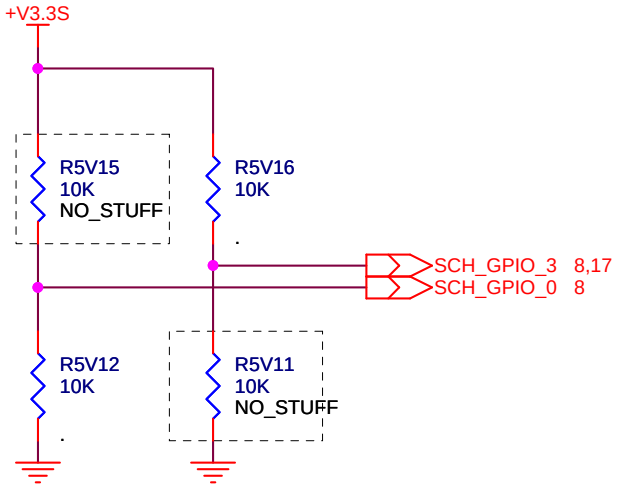
J8D3 default: Open



Note: Test Only
Do Not Populate

Poulsbo strapping table

5..8,11,12,14..18,20..22,24,25,27,29,31,34,35,38,40,41,43..46,49..51,57,58



CMC Base Address

SCH_GPIO_3	SCH_GPIO_0	Address
0	0	0xFFFB0000
0	1	0xFFFC0000
1	0	0xFFFD0000 (Default)
1	1	0xFFFE0000

Crown Beach Intel Confidential

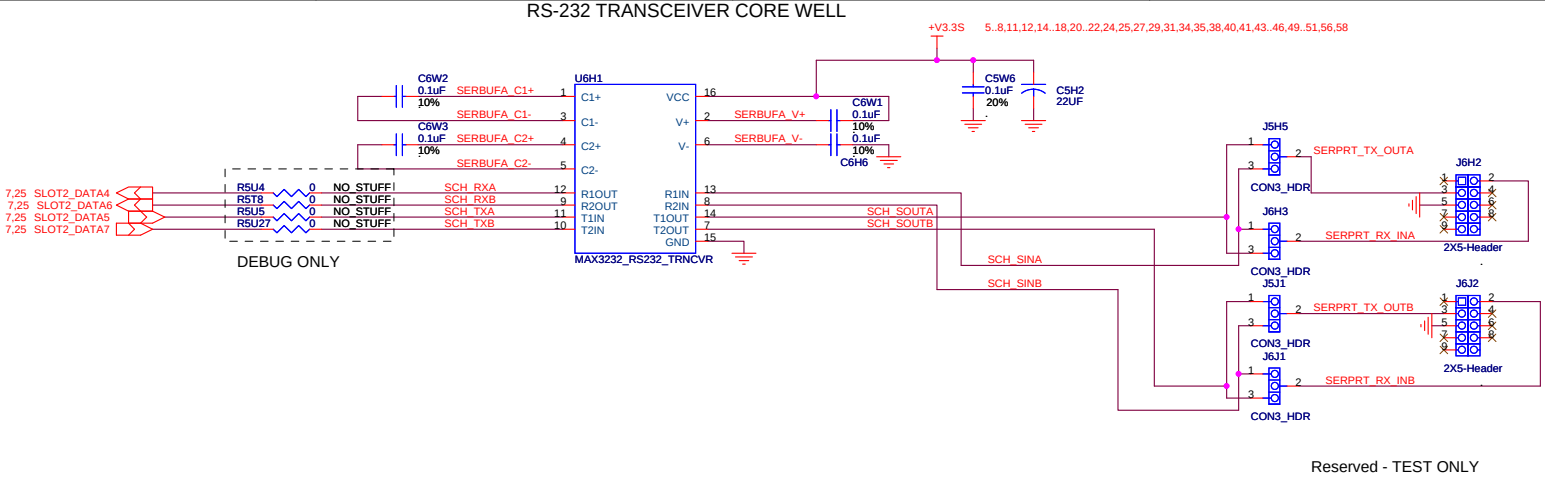
Title: Validation Hooks 1

Size: A | Document Number | Rev: 1.5

Date: Friday, November 16, 2007 | Sheet 56 of 64

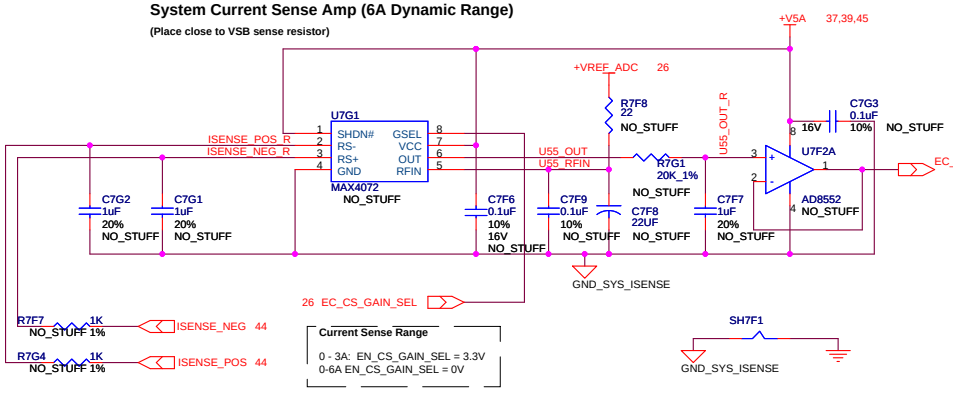
RS-232 TRANSCEIVER CORE WELL

RS232 PORT MODE	
Setting	Mode
Both 1-2 (default)	Data Communications Equipment (Use a normal cable)
Both 2-3	Data Terminal Equipment (Use a null modem cable)



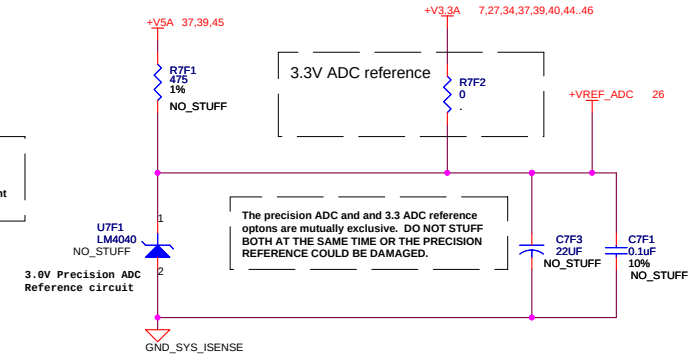
System Current Sense Amp (6A Dynamic Range)

(Place close to VSB sense resistor)



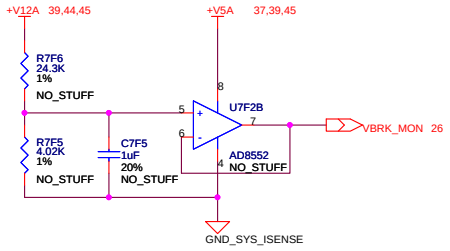
Embedded Controller ADC Reference

(Place close to the EC)



System Voltage Monitor

(Place close to VSB sense resistor)



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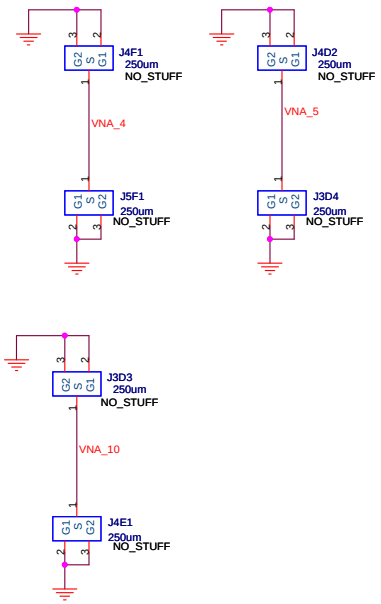
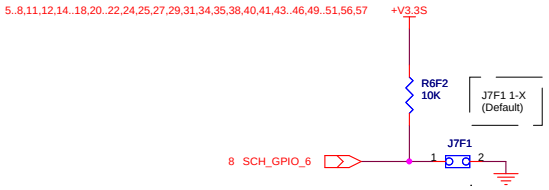
TEST COUPONS





Reserved - TEST ONLY

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Title: Validation Hooks 3		
Size: A	Document Number	Rev: 1.5
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